GENEVA

CPU : MEROM
Chip Set : SANTAROSA CHIPSET
Remarks : Mobility Platform

Model Name : GENEVA
PBA Name : MAIN
PCB Code : BA41-XXXXX
Dev. Step : PV2
Revision : 1.0
T.R. Date :

DRAW	CHECK	APPROVAL

Table of Contents

DRAW: SUN XIAO	DATE: 6/26/2007	TITLE: Gevena	SAMSUNG ELECTRONICS
CHECK: WUSHIJIANG	DEV. STEP: PV2	MILAN	
APPROVAL: KEVIN LEE	REV: 1.0	COVER	PART NO.: BA41-XXXXX
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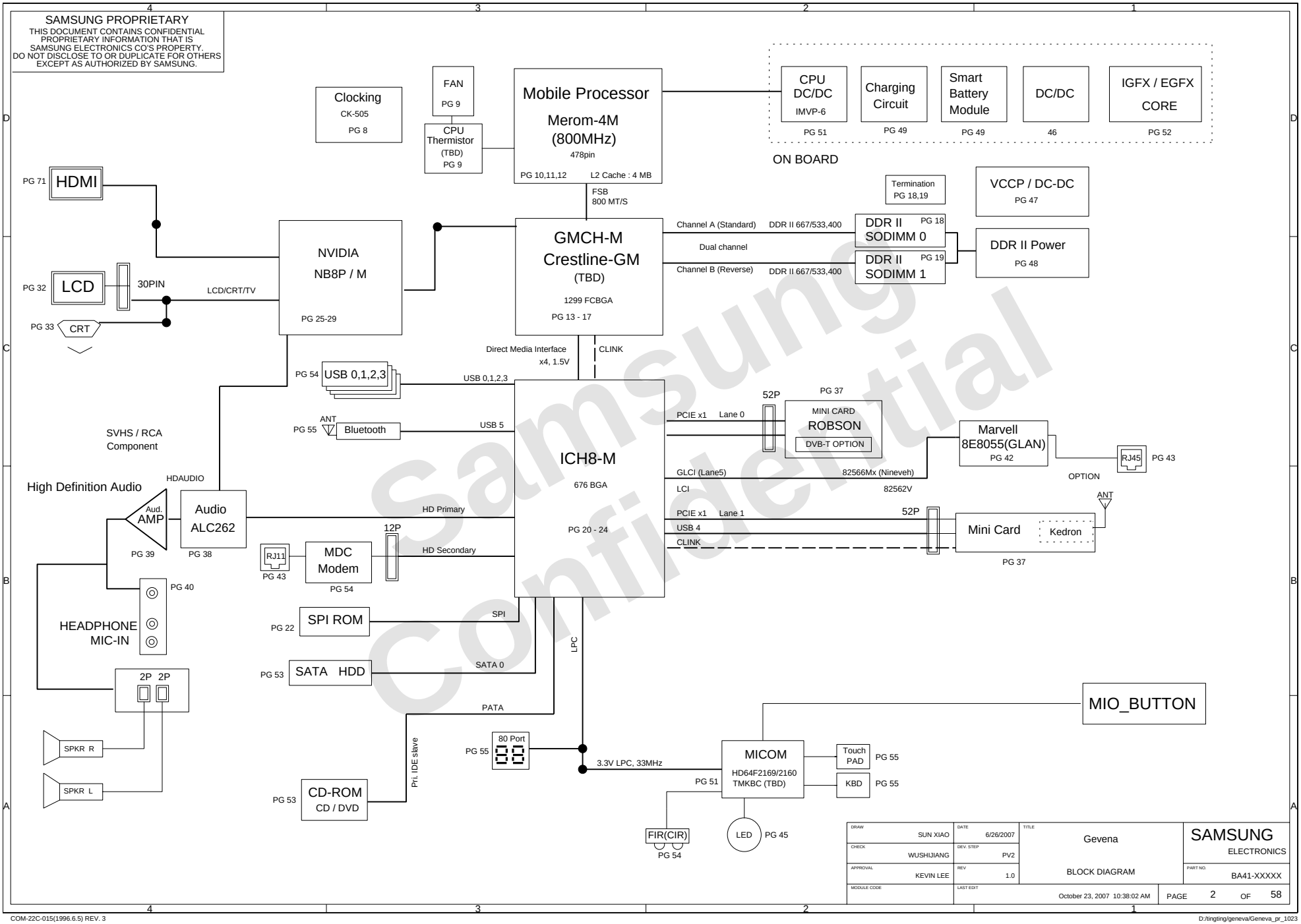

DRAW: SUN XIAO	DATE: 6/26/2007	TITLE: Gevena	SAMSUNG ELECTRONICS
CHECK: WUSHIJIANG	DEV. STEP: PV2		
APPROVAL: KEVIN LEE	REV: 1.0	BLOCK DIAGRAM	PART NO.: BA41-XXXXX
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BOARD INFORMATION

SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

PCI Devices

Devices	IDSEL#	REQ/GNT#	Interrupts
Cardbus	AD25	3	B,C,D
DT PCI SLOT	AD22	1	B,C,D,C
MiniPCI SLOT	AD23	2	A,B
USB	AD29(internal)	-	USB2.0 #0 (USB0) : A USB2.0 #1 (USB1) : D USB2.0 #2 (USB4) : C USB2.0 #3 (USB5) : E USB2.0 #4 (EHCI) : H
Hub to PCI	AD30(internal)	-	-
LPC bridge/IDE/AC97/SMBUS	AD31(internal)	-	B
Internal MAC	AD24(internal)	-	E
AC Link	-	-	B
GLAN	-	-	F

Voltage Rails

VDC	Primary DC system power supply (7 to 21V)
VCC_CORE	Core Voltage for CPU
MCH_CORE	Core Voltage for CPU
ICH_CORE	Core Voltage for CPU
P1.05V (VCCP)	VTT for CPU, Crestline & ICH8-M
P1.05V_M	1.05V switched power rail for ME (on in M0/M1)
P1.25V_M	1.25V switched power rail for ME (on in M0/M1)
P3.3V_M	3.3V switched power rail for ME (on in M0/M1)
P3.3V_A	3.3V always power rail (by KBC3_ALWS_ON)
MICOM_P3V	3.3V always power rail (for Micom)
LAN_3.3V	3.3V always power rail (for LAN)
P1.5V	1.5V switched off power rail (off in S3-S5)
P1.5V_AUX	1.5V switched on power rail
P2.5V	2.5V switched off power rail (off in S3-S5)
P1.8V	1.8V switched off power rail (off in S3-S5)
P1.8V_AUX	1.8V power rail for DDR
P0.9V	0.9V power rail for DDR
P3.3V	3.3V switched off power rail (off in S3-S5)
P3.3V_AUX	3.3V switched on power rail
P5V	5.0V switched off power rail (off in S3-S5)
P5V_AUX	5.0V switched on power rail

USB PORT Assign

PORT #	ASSIGNED TO
0	SYSTEM PORT 0
1	SYSTEM PORT 1
2	DMB
3	Expresas Card
4	DOCKING PORT 0
5	Bluetooth
6	Mini PCI Express
7	Aux Display
8	Test Port (RSVD)
9	WWAN/WIBRO (TBD)

PCI Express Assign

PORT #	ASSIGNED TO
0	PCIE x1 Slot
1	Mini Card (Golan)
2	Mini Card (WIBRO : RSVD)
3	Expresas Card
4	DOCKING PORT 0
5	GLAN

Crystal / Oscillator

TYPE	FREQUENCY	DEVICE	USAGE
Crystal	32.768KHz	ICH8-M	Real Time Clock
Crystal	10MHz	MICOM	HD64F2169/2160
Crystal	14.318MHz	CLOCK-Generator	CK-505
Crystal	24.576MHz	Cardbus Controller	1394
Crystal	25MHz	LAN	Intel LAN
Crystal	27MHz (TBD)	VIDEO	PEG
Crystal	24.576MHz (TBD)	HD Audio	Audio

LCD Pannel Detect (TBD)

Devices	Resolution	PANNEL_DETECT_0

I^{2}C / SMB Address

Devices	Address	Hex	Bus
ICH8-m	Master	-	SMBUS Master
CPU Thermal Sensor	1001 110x	9Ch	Thermal Sensor
SODIMM0	1010 000x	A0h	-
SODIMM1	1010 010x	A4h	-
Thermal Sensor on SODIMM0	0011 000x	30h	-
Thermal Sensor on SODIMM1	0011 010x	34h	-
CK-505M (Clock Generator)	1101 001x	D2h	Clock, Unused Clock Output Disable
DB400 (PCI Express Clocks)	1101 110x	DCh	Clock Buffer for PCI Express
TBD	0100 1100	4Ch	Thermal Sensor
TBD : (LVDS BackLight Inverter)	0101 1000	58h	-
TBD : (ALS)	0111 0010	72h	Ambient Light Sensor
TBD : (AUX DISPLAY)	0011 110x	3Ch	EMA
LAN	1100 1000	C8h	82566
PCI Express Docking	TBD	TBD	TBD
TPM	TBD	TBD	TBD

REVISION HISTORY

See rev notes for more information.

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CHECK: WUSHIJIANG	DEV. STEP: PV2		
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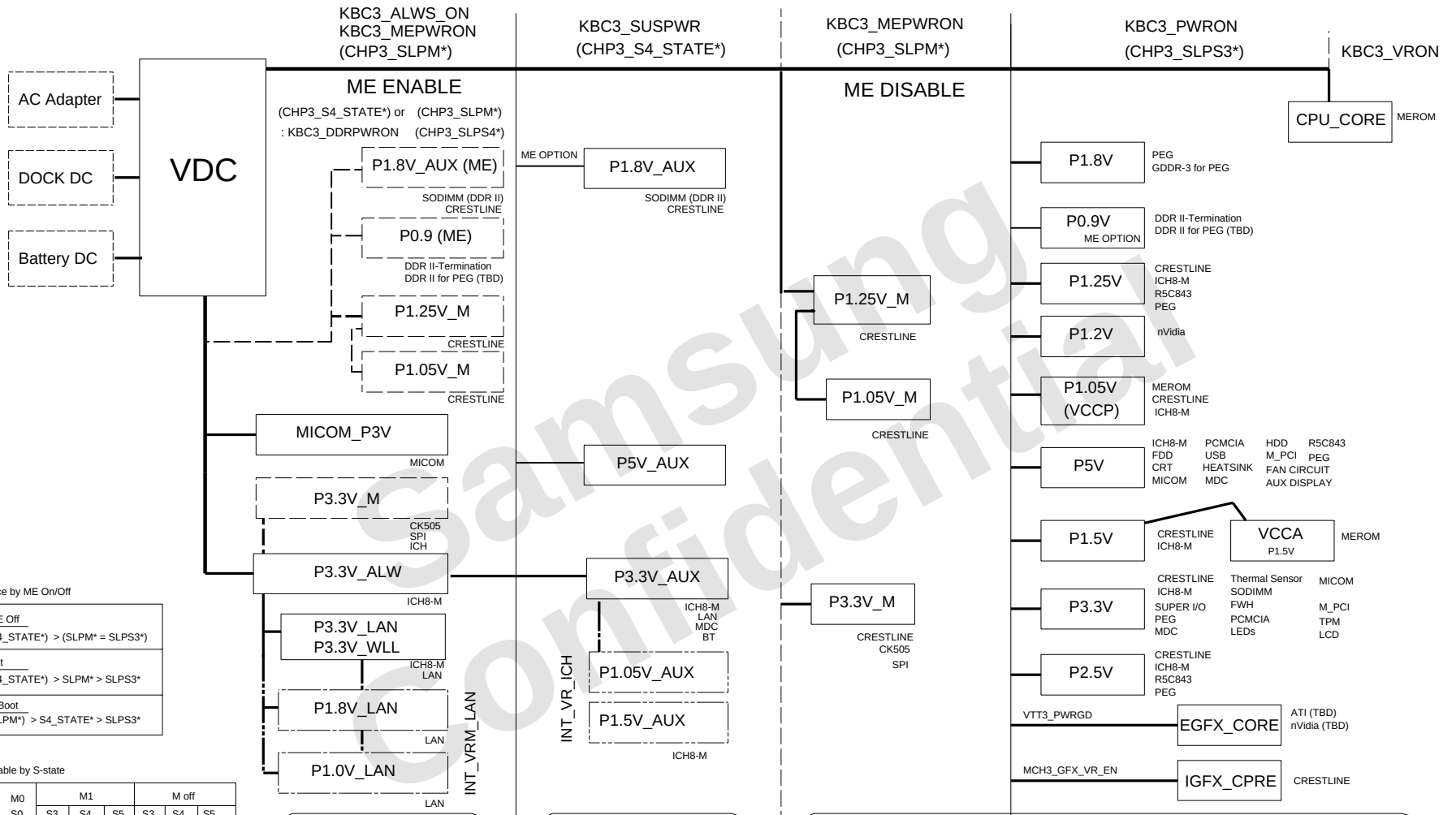
POWER DIAGRAM



Power Sequence by ME On/Off

Host Boot / ME Off (SLPS4* = S4_STATE*) > (SLPM* = SLPS3*)
Host / ME Boot (SLPS4* = S4_STATE*) > SLPM* > SLPS3*
Host S5 / ME Boot (SLPS4* = SLPM*) > S4_STATE* > SLPS3*

Power On/Off Table by S-state

Rail / State	M0	M1			M off		
	S0	S3	S4	S5	S3	S4	S5
+V*A(LWS) +V*LAN	ON	ON	ON	ON	ON	ON	ON
+1.8V_AUX	ON	ON	ON	ON	ON	—	—
+0.9V	ON	ON	ON	ON	—	—	—
+V*AUX	ON	ON	—	—	ON	—	—
+V* M	ON	ON	ON	ON	—	—	—
+V* (CORE)	ON	—	—	—	—	—	—

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CHECK: WUSHIJIANG	DEV. STEP: PV2		
APPROVAL: KEVIN LEE	REV: 1.0	POWER DIAGRAM	PART NO.: BA41-XXXXX
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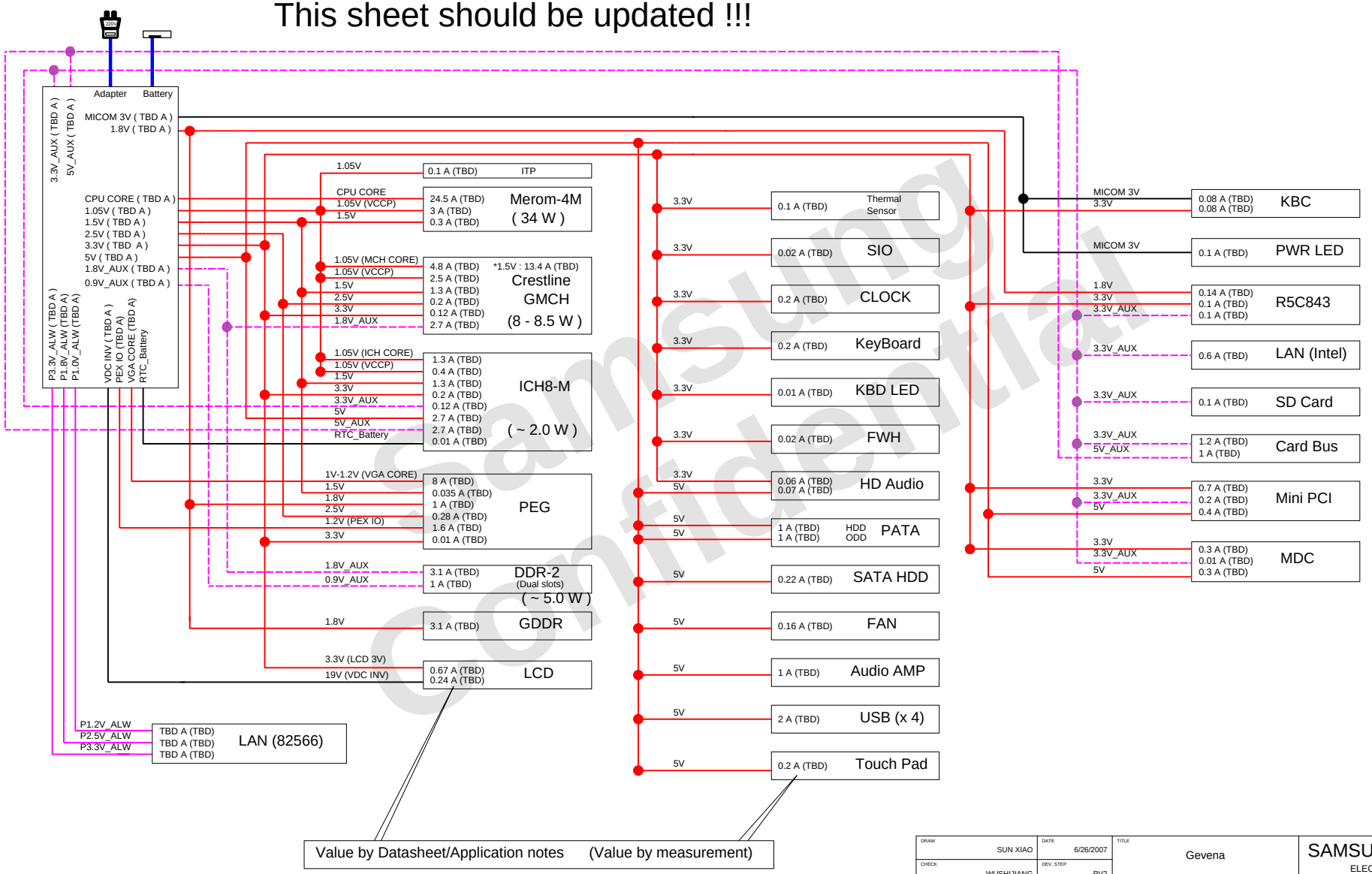
POWER RAILS ANALYSIS

Rev. 0.5

This sheet should be updated !!!



DRAW: SUN XIAO	DATE: 6/26/2007	TITLE: Gevena	SAMSUNG ELECTRONICS
CHECK: WUSHIJIANG	DEV. STEP: PV2		
APPROVAL: KEVIN LEE	REV: 1.0	POWER RAILS	PART NO.: BA41-XXXXX
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POWER SEQUENCE Rev. 0.5

TO BE UPDATED!!

Host Boot / ME Off
(SLPS4* = S4_STATE*) > (SLPM* = SLPS3*)
M-1) KBC3_DDR_PWRON (TBD) = 8) KBC3_SUSPWR
M-2) KBC3_ME_PWRON = 15) KBC3_PWRON

Host / ME Boot
(SLPS4* = S4_STATE*) > SLPM* > SLPS3*

Host S5 / ME Boot
(SLPS4* = SLPM*) > S4_STATE* > SLPS3*

RTC Battery — 1) VCC_RTC, CHP3_RTCRST

POWER S/W (DC/DC B'd) — 4) POWER_SW*

KBC
10) CHP3_SLPS5*
11) CHP3_SLPS4*
12) CHP3_SLPSM*
13) CHP3_S4_STATE*
14) CHP3_SLPS3*
18) KBC3_PWRGD (Test Option)
M-1) KBC3_DDR_PWRON
M-2) KBC3_ME_PWRON
8) KBC3_SUSPWR
15) KBC3_PWRON
19) KBC3_VRON

ICH8-M (Sheet 22-25)
16) ICH_CORE (P1.05V)
6) P3.3V_LAN(A), 9) P3.3V_AUX
PRTC, PRTC
LAN100_SLP, INTVRMEN
7) P1.05V_AUX, 7) P1.5V_AUX
VRMPWRGD
PWROK
CL_PWROK
23) CLK3_PWRGD
9-M) P3.3V_M
CHP3_VRMPWRGD
26) VRM3_CPU_PWRGD
22) CLK3_PWRGD*_INV
27) CHP3_PWROK
17) CHP3_ME_PWROK
16-PG) VTT3_PWRGD
9-PG) 1.8V_AUX_PWRGD
28) CPU1_PWRGDCPU
29) PLT3_RST*
29) PCI3_RST*

CK-505 (Sheet 8)
9-M) ME Host Clock
24) Clock Running

CPU VRM (DC/DC B'd)
PG-2) VTT3_PWRGD
18) KBC3_PWRGD
19) KBC3_VRON
20) KBC3_ALL_PWRGD
21) CLK3_PWRGD*
26) VRM3_CPU_PWRGD
25) VCC_CORE

CPU (Sheet 10-12) (Test Option)
28) CPU1_PWRGDCPU
16) P1.5V
16) P1.05V
30) CPU1_CPURST*

GMCH (Sheet 15-19)
27) CHP3_PWROK
17) CHP3_ME_PWROK
PWROK
CL_PWROK
29) PLT3_RST*
9-M) P1.05V_M
9-M) P1.25V_M
16) MCH_CORE
16) GFX_CORE
9) P1.8V_AUX
16) P1.05V
16) P3.3V

Thermal Monitor (Sheet 14)

MICOM_P3V

Adapter / Battery — AC_DC / Battery — MAX 8724
2) VDC
5) KBC3_ALWS_ON
8) KBC3_SUSPWR
M-2) KBC3_ME_PWRON
15) KBC3_PWRON

MIC5219 — 16) P2.5V
LT1930 — 16) P12V
GFX VR — 16) GFX_CORE

DDR2 POWER
MAX8632 (Sheet 50)
8) KBC3_SUSPWR or M-2) KBC3_ME_PWRON
2) VDC
M-1) KBC3_DDR_PWRON (Test Option)
8) KBC3_SUSPWR
M-2) KBC3_ME_PWRON
9) P1.8V_AUX
9) 0.9V
9-PG) 1.8V_AUX_PWRGD

TPS5130
2) VDC
M-2) KBC3_ME_PWRON
15) KBC3_PWRON
9-M) P1.05V_M
9-M) P1.25V_M
16) P1.5V
16) P1.2V
16-PG) VTT3_PWRGD

P3.3V_LAN & P5V_AUX
MAX 1999
9) P5V_AUX
6) P3.3V_LAN

FDS6680A (Sheet 40) — 9-M) P3.3V_M
FDS6680A (Sheet 40) — 9) P3.3V_AUX
FDS4435 (Sheet 40) — 9) P5V_AUX → 16) P5V
FDS6680A (Sheet 40) — 9) P3.3V_AUX → 16) P3.3V
FDS6680A (Sheet 40) — 9) P1.8V_AUX → 16) P1.8V
FDS6680A (Sheet 40) — 9-M) P1.25V_M → 16) P1.25V
FDS6680A (Sheet 40) — 9-M) P1.05V_M → 16) P1.05V

DDR2 Memory (Sheet 20-21)
9) P1.8V_AUX
9) P0.9V
9-M) P3.3V_M

PCIe Devices
16) P3.3V
16) P1.8V
16) P1.5V

PEG
16) P1.2V
2) VDC
16) P3.3V

PCI Devices
16) P3.3V
16) P1.8V
16) P1.5V
29) PCI3_RST*

LOM Nineveh (Sheet 46-47)
7) P1.0V_LAN
7) P1.8V_LAN

BCP69 (Sheet 46)

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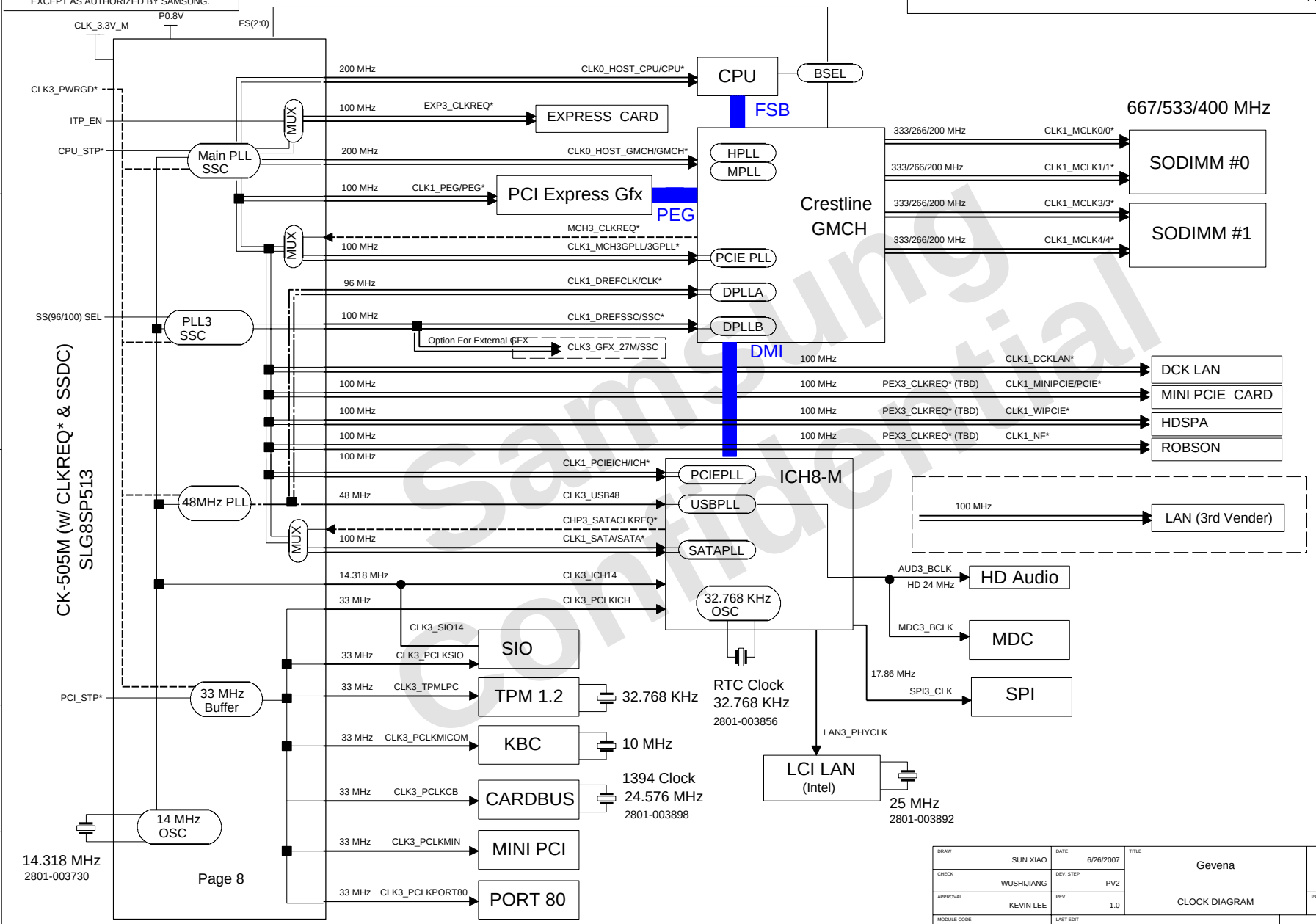
CLOCK DISTRIBUTION

Rev. 0.8



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CHECK: WUSHIJIANG	DEV. STEP: PV2		
APPROVAL: KEVIN LEE	REV: 1.0	CLOCK DIAGRAM	PART NO.: BA41-XXXXX
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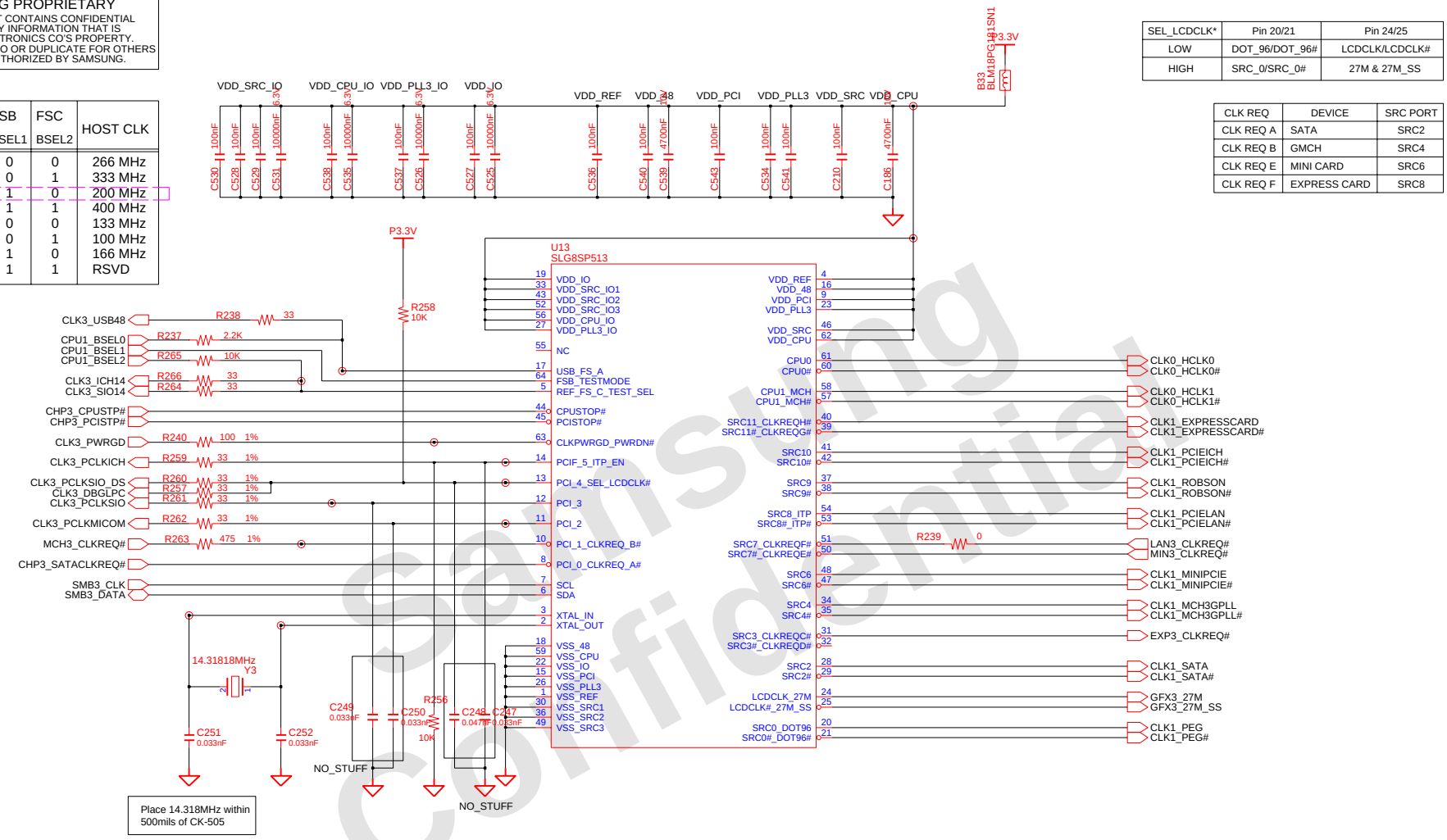
FSA BSEL0	FSB BSEL1	FSC BSEL2	HOST CLK
0	0	0	266 MHz
0	0	1	333 MHz
0	1	0	200 MHz
0	1	1	400 MHz
1	0	0	133 MHz
1	0	1	100 MHz
1	1	0	166 MHz
1	1	1	RSVD

SEL_LCDCLK*	Pin 20/21	Pin 24/25
LOW	DOT_96/DOT_96#	LCDCLK/LCDCLK#
HIGH	SRC_0/SRC_0#	27M & 27M_SS

CLK REQ	DEVICE	SRC PORT
CLK REQ A	SATA	SRC2
CLK REQ B	GMCH	SRC4
CLK REQ E	MINI CARD	SRC6
CLK REQ F	EXPRESS CARD	SRC8



DRAW: SUN XIAO	DATE: 6/26/2007	TITLE: Gevena CLOCK GENERATOR CK-505	SAMSUNG ELECTRONICS
CHECK: WUSHIJIANG	DEV. STEP: PV2		
APPROVAL: KEVIN LEE	REV: 1.0		PART NO.: BA41-XXXXX
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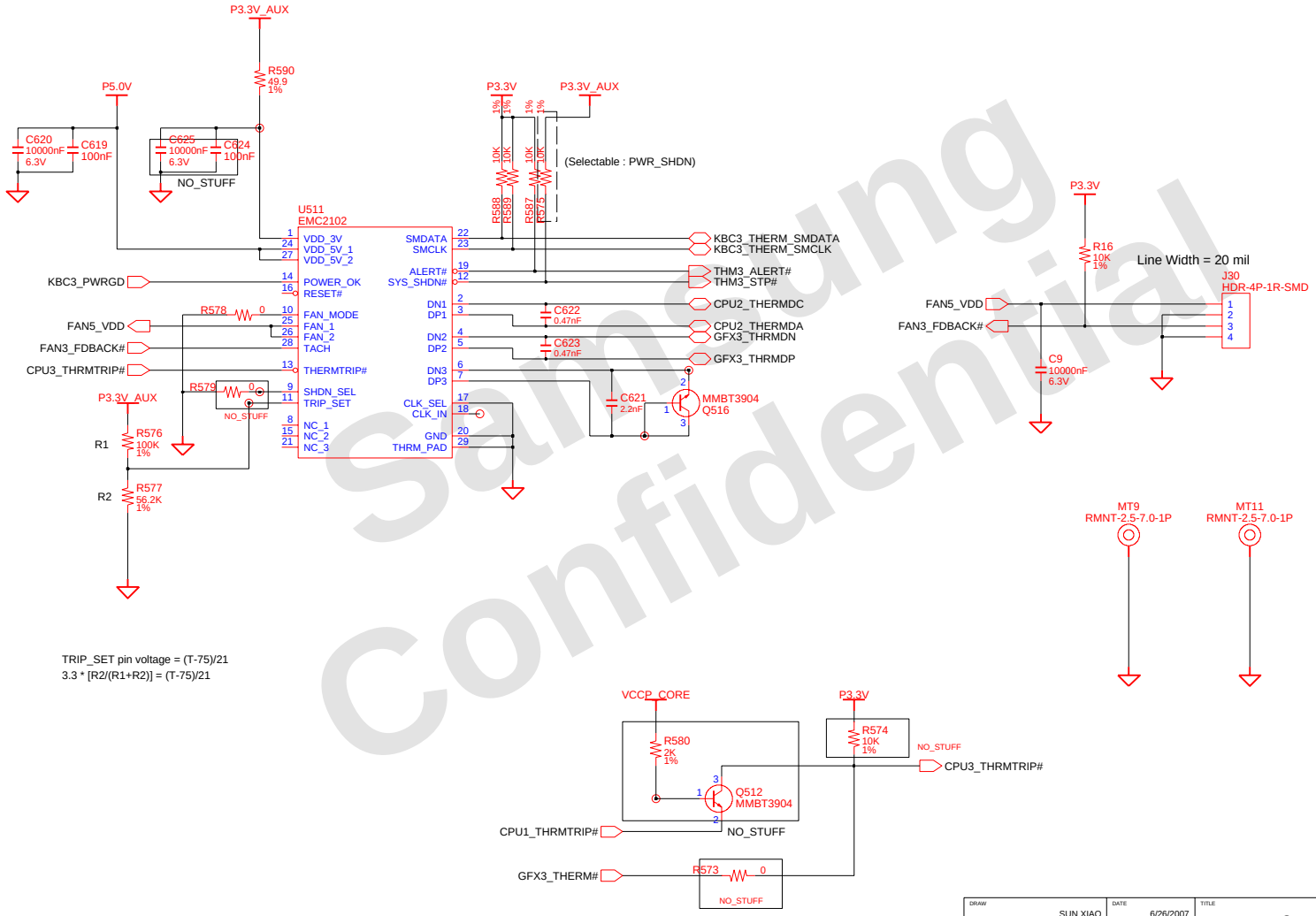
THERMAL SENSOR & FAN CONTROL



DRAW: SUN XIAO	DATE: 6/26/2007	TITLE: Gevena THERMAL BLOCK THERMAL & FAN CONTROL	SAMSUNG ELECTRONICS
CHECK: WUSHIJIANG	DEV. STEP: PV2		
APPROVAL: KEVIN LEE	REV: 1.0		PART NO.: BA41-XXXXX
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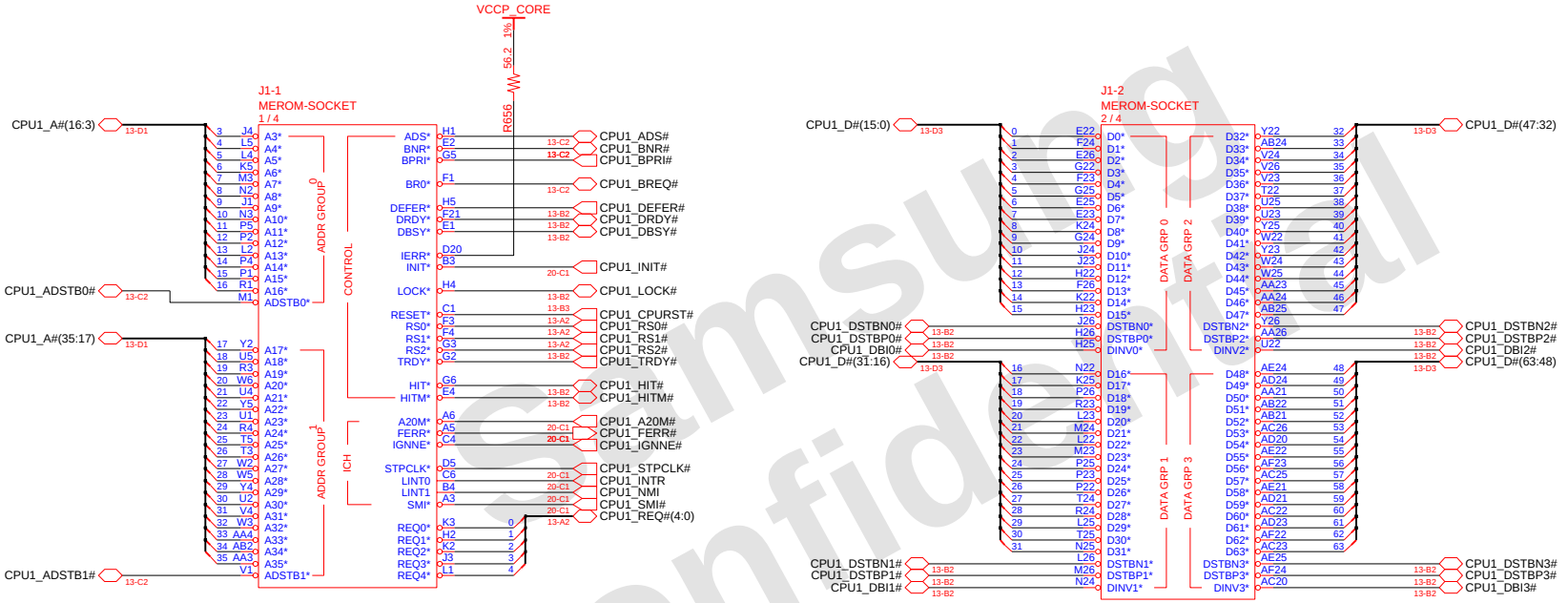
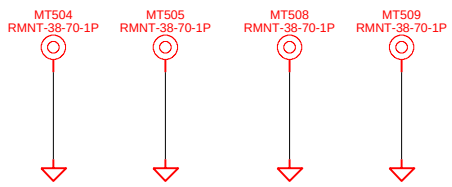


CPU CONNECTOR PART NUMBER 3704-001153



DRAW: SUN XIAO	DATE: 6/26/2007	TITLE: Gevena CPU MEROM(1/3)	SAMSUNG ELECTRONICS
CHECK: WUSHIJIANG	DEV. STEP: PV2		
APPROVAL: KEVIN LEE	REV: 1.0		PART NO.: BA41-XXXXX
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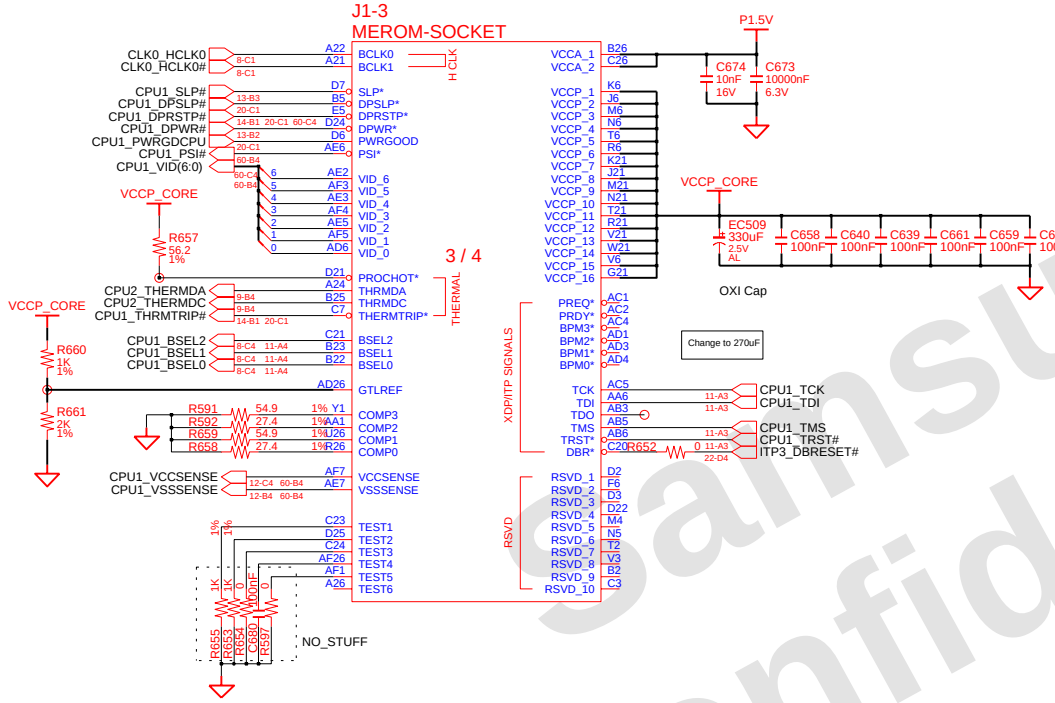
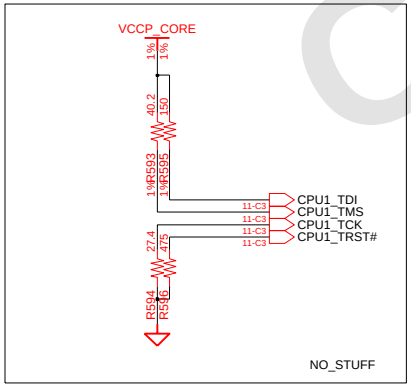


ITP DISABLE



CPU Core Voltage Table

IMVP-6

Active Mode VID(6:0)	Voltage	Active/Deeper Sleep Dual Mode Region VID(6:0)	Voltage	Deeper Sleep/Extended Deeper Sleep Dual Mode Region VID(6:0)	Voltage
0 0 0 0 0 0 0	1.5000 V	0 1 0 1 0 0 0	1.0000 V	1 0 1 0 0 0 1	0.4875 V
0 0 0 0 0 0 1	1.4875 V	0 1 0 1 0 0 1	0.9875 V	1 0 1 0 0 1 0	0.4750 V
0 0 0 0 0 1 0	1.4750 V	0 1 0 1 0 1 0	0.9750 V	1 0 1 0 0 1 1	0.4625 V
0 0 0 0 0 1 1	1.4625 V	0 1 0 1 0 1 1	0.9625 V	1 0 1 0 1 0 0	0.4500 V
0 0 0 0 1 0 0	1.4500 V	0 1 0 1 1 0 0	0.9500 V	1 0 1 0 1 0 1	0.4375 V
0 0 0 0 1 0 1	1.4375 V	0 1 0 1 1 0 1	0.9375 V	1 0 1 0 1 1 0	0.4250 V
0 0 0 0 1 1 0	1.4250 V	0 1 0 1 1 1 0	0.9250 V	1 0 1 0 1 1 1	0.4125 V
0 0 0 0 1 1 1	1.4125 V	0 1 0 1 1 1 1	0.9125 V	1 0 1 1 0 0 0	0.4000 V
0 0 0 1 0 0 0	1.4000 V	0 1 1 0 0 0 0	0.9000 V	1 0 1 1 0 0 1	0.3875 V
0 0 0 1 0 0 1	1.3875 V	0 1 1 0 0 0 1	0.8875 V	1 0 1 1 0 1 0	0.3750 V
0 0 0 1 0 1 0	1.3750 V	0 1 1 0 0 1 0	0.8750 V	1 0 1 1 0 1 1	0.3625 V
0 0 0 1 0 1 1	1.3625 V	0 1 1 0 0 1 1	0.8625 V	1 0 1 1 1 0 0	0.3500 V
0 0 0 1 1 0 0	1.3500 V	0 1 1 0 1 0 0	0.8500 V	1 0 1 1 1 0 1	0.3375 V
0 0 0 1 1 0 1	1.3375 V	0 1 1 0 1 0 1	0.8375 V	1 0 1 1 1 1 0	0.3250 V
0 0 0 1 1 1 0	1.3250 V	0 1 1 0 1 1 0	0.8250 V	1 0 1 1 1 1 1	0.3125 V
0 0 0 1 1 1 1	1.3125 V	0 1 1 0 1 1 1	0.8125 V	1 1 0 0 0 0 0	0.3000 V
0 0 1 0 0 0 0	1.3000 V	0 1 1 1 0 0 0	0.8000 V	1 1 0 0 0 0 1	0.2875 V
0 0 1 0 0 0 1	1.2875 V	0 1 1 1 0 0 1	0.7875 V	1 1 0 0 0 1 0	0.2750 V
0 0 1 0 0 1 0	1.2750 V	0 1 1 1 0 1 0	0.7750 V	1 1 0 0 0 1 1	0.2625 V
0 0 1 0 0 1 1	1.2625 V	0 1 1 1 0 1 1	0.7625 V	1 1 0 0 1 0 0	0.2500 V
0 0 1 0 1 0 0	1.2500 V	0 1 1 1 1 0 0	0.7500 V	1 1 0 0 1 0 1	0.2375 V
0 0 1 0 1 0 1	1.2375 V	0 1 1 1 1 0 1	0.7375 V	1 1 0 0 1 1 0	0.2250 V
0 0 1 0 1 1 0	1.2250 V	0 1 1 1 1 1 0	0.7250 V	1 1 0 0 1 1 1	0.2125 V
0 0 1 0 1 1 1	1.2125 V	0 1 1 1 1 1 1	0.7125 V	1 1 0 1 0 0 0	0.2000 V
0 0 1 1 0 0 0	1.2000 V	1 0 0 0 0 0 0	0.7000 V	1 1 0 1 0 0 1	0.1875 V
0 0 1 1 0 0 1	1.1875 V	1 0 0 0 0 0 1	0.6875 V	1 1 0 1 0 1 0	0.1750 V
0 0 1 1 0 1 0	1.1750 V	1 0 0 0 0 1 0	0.6750 V	1 1 0 1 0 1 1	0.1625 V
0 0 1 1 0 1 1	1.1625 V	1 0 0 0 0 1 1	0.6625 V	1 1 0 1 1 0 0	0.1500 V
0 0 1 1 1 0 0	1.1500 V	1 0 0 0 1 0 0	0.6500 V	1 1 0 1 1 0 1	0.1375 V
0 0 1 1 1 0 1	1.1375 V	1 0 0 0 1 0 1	0.6375 V	1 1 0 1 1 1 0	0.1250 V
0 0 1 1 1 1 0	1.1250 V	1 0 0 0 1 1 0	0.6250 V	1 1 0 1 1 1 1	0.1125 V
0 0 1 1 1 1 1	1.1125 V	1 0 0 0 1 1 1	0.6125 V	1 1 1 0 0 0 0	0.1000 V
0 1 0 0 0 0 0	1.1000 V	1 0 0 1 0 0 0	0.6000 V	1 1 1 0 0 0 1	0.0875 V
0 1 0 0 0 0 1	1.0875 V	1 0 0 1 0 0 1	0.5875 V	1 1 1 0 0 1 0	0.0750 V
0 1 0 0 0 1 0	1.0750 V	1 0 0 1 0 1 0	0.5750 V	1 1 1 0 0 1 1	0.0625 V
0 1 0 0 0 1 1	1.0625 V	1 0 0 1 0 1 1	0.5625 V	1 1 1 0 1 0 0	0.0500 V
0 1 0 0 1 0 0	1.0500 V	1 0 0 1 1 0 0	0.5500 V	1 1 1 0 1 0 1	0.0375 V
0 1 0 0 1 0 1	1.0375 V	1 0 0 1 1 0 1	0.5375 V	1 1 1 0 1 1 0	0.0250 V
0 1 0 0 1 1 0	1.0250 V	1 0 0 1 1 1 0	0.5250 V	1 1 1 0 1 1 1	0.0125 V
0 1 0 0 1 1 1	1.0125 V	1 0 0 1 1 1 1	0.5125 V	1 1 1 1 0 0 0	0.0000 V
		1 0 1 0 0 0 0	0.5000 V	1 1 1 1 0 0 1	0.0000 V
				1 1 1 1 0 1 0	0.0000 V
				1 1 1 1 0 1 1	0.0000 V
				1 1 1 1 1 0 0	0.0000 V
				1 1 1 1 1 0 1	0.0000 V
				1 1 1 1 1 1 0	0.0000 V
				1 1 1 1 1 1 1	0.0000 V

Active	
DPRSLPVR	0
DPRSTP*	1
PSI2*	0 or 1

Deeper Slp	
DPRSLPVR	1
DPRSTP*	0
PSI2*	0 or 1

*"1111111" : 0V power good asserted.

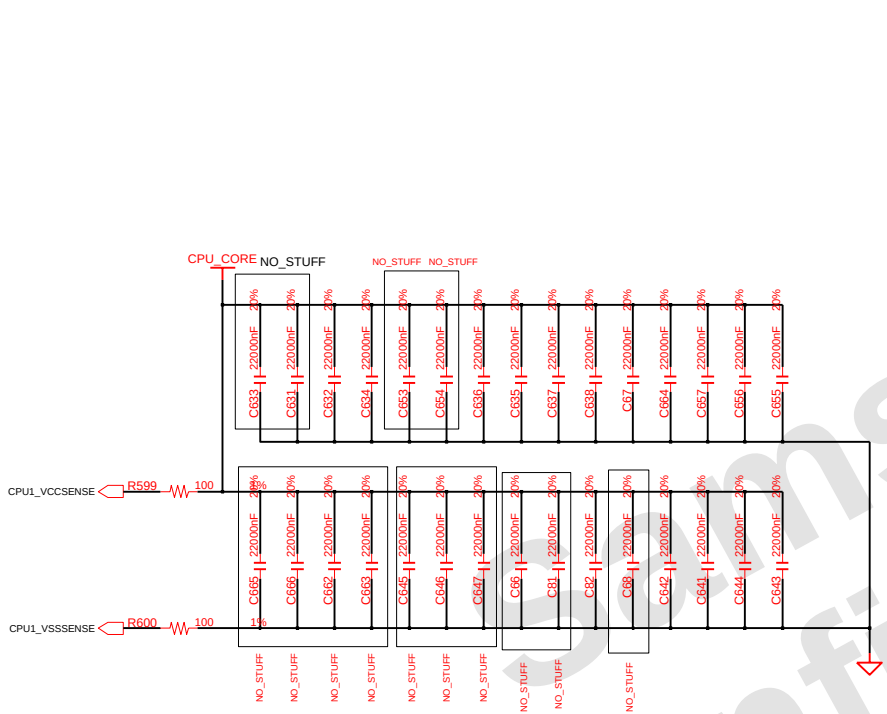
*Yonah Processor (2.33 GHz / 800 MHz : TBD)

GTLREF : Keep the Voltage divider within 0.5" of the first GTLREF0 pin with Zo=55ohm trace. Minimize coupling of any switching signals to this net.

COMP0,2(COMP1,3) should be connected with Zo=27.4ohm(55ohm) trace shorter than 1/2" to their respective Banias socket pins.

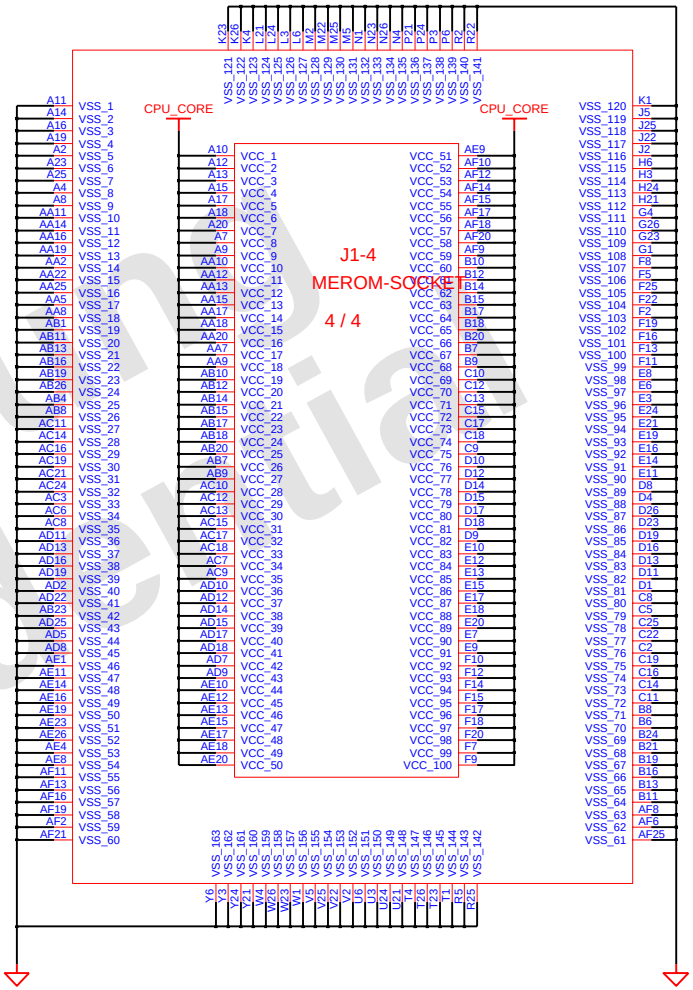
GND test points within 100mil of the VCC/VSSsense at the end of the line. Route the VCC/VSSsense as a Zo=55ohm traces with equal length. Observe 3:1 spacing b/w VCC/VSSsense lines and 25mil away (preferred 50mil) from any other signal. And GND via 100mil away from each of the VCC/VSS test point vias.

DRAW: SUN XIAO	DATE: 6/26/2007	TITLE: Gevena CPU MEROM(2/3)	SAMSUNG ELECTRONICS
CHECK: WUSHIJIANG	DEV. STEP: PV2		
APPROVAL: KEVIN LEE	REV: 1.0		PART NO.: BA41-XXXXX
MODULE CODE	LAST EDIT: October 23, 2007 10:38:02 AM	PAGE 11 OF 58	

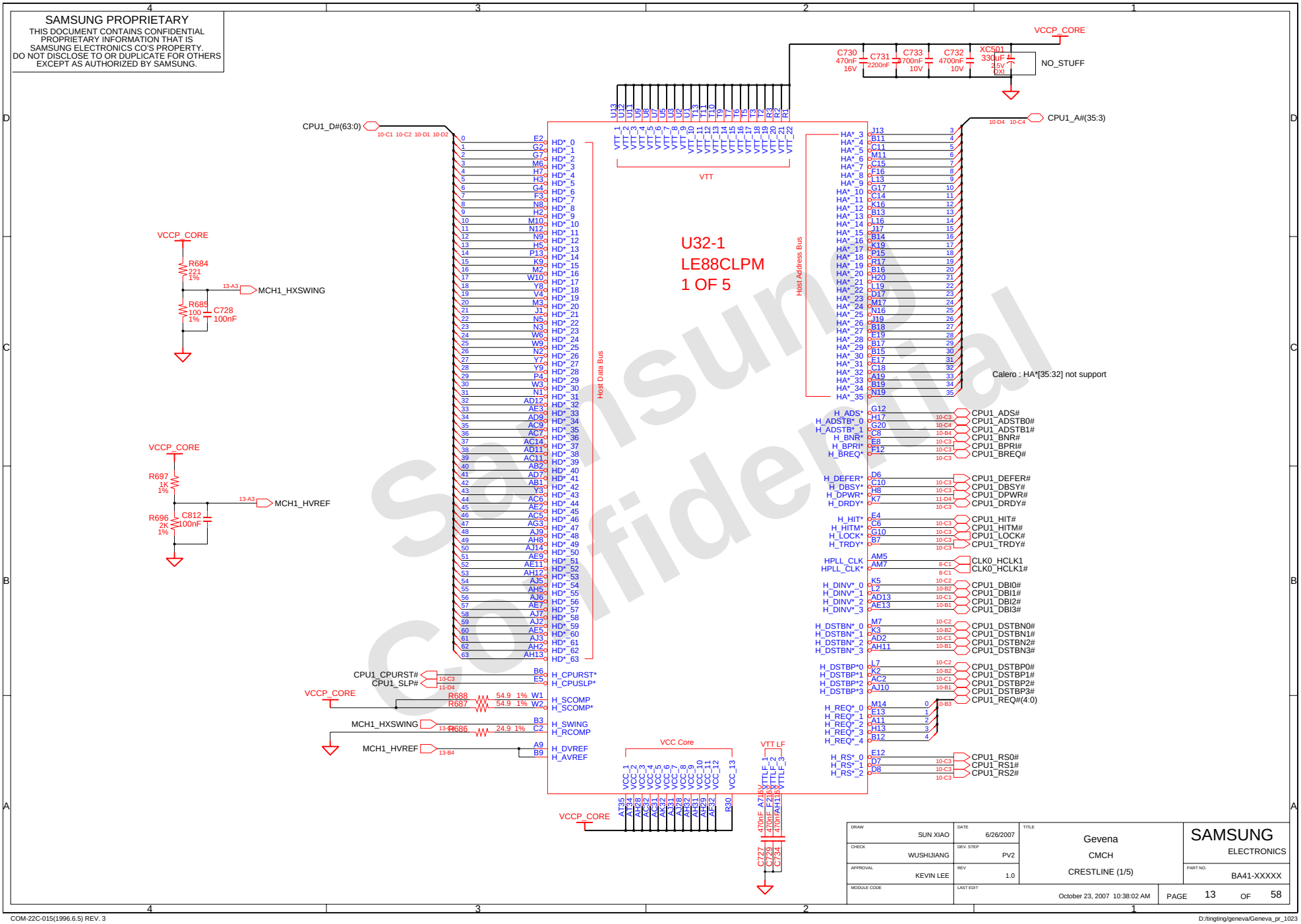


6x 330 uF : CPU VR side

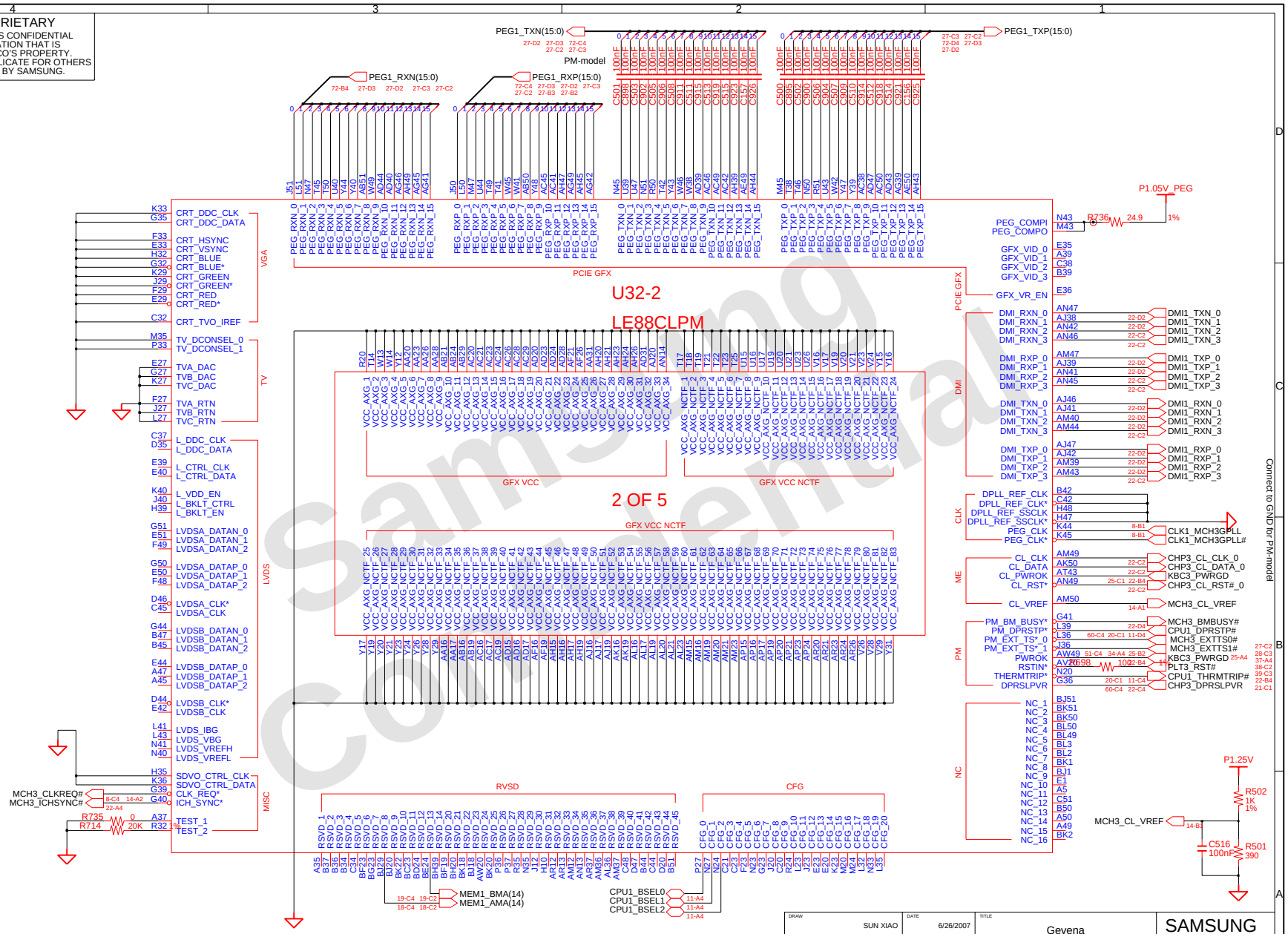
Be Caution the placement of decap!!



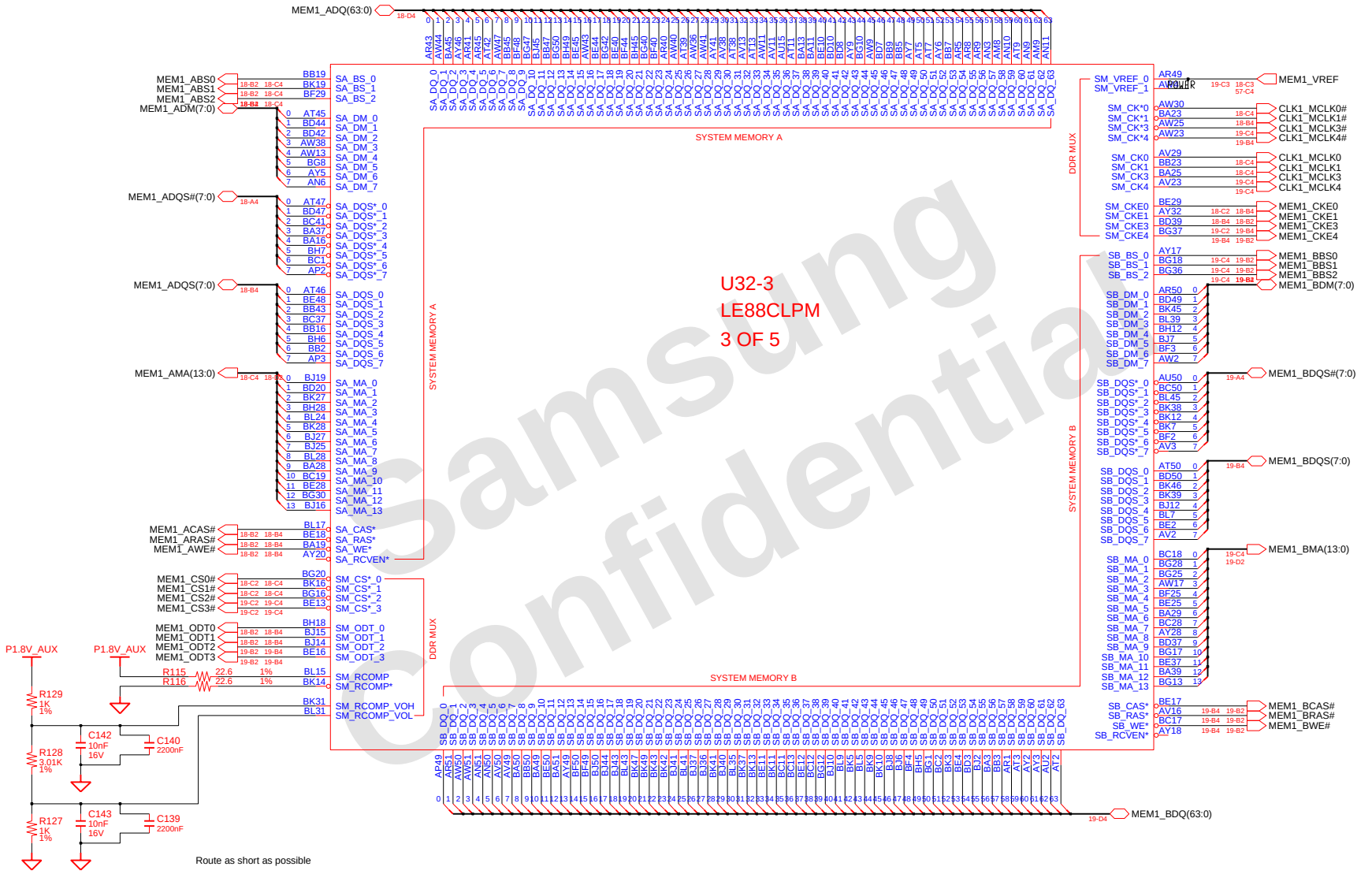
DRAW: SUN XIAO	DATE: 6/26/2007	TITLE: Gevena / CPU / MEROM(3/3)	SAMSUNG ELECTRONICS
CHECK: WUSHIJIANG	DEV. STEP: PV2		
APPROVAL: KEVIN LEE	REV: 1.0		PART NO.: BA41-XXXXX
MODULE CODE	LAST EDIT: October 23, 2007 10:38:02 AM	PAGE 12 OF 58	



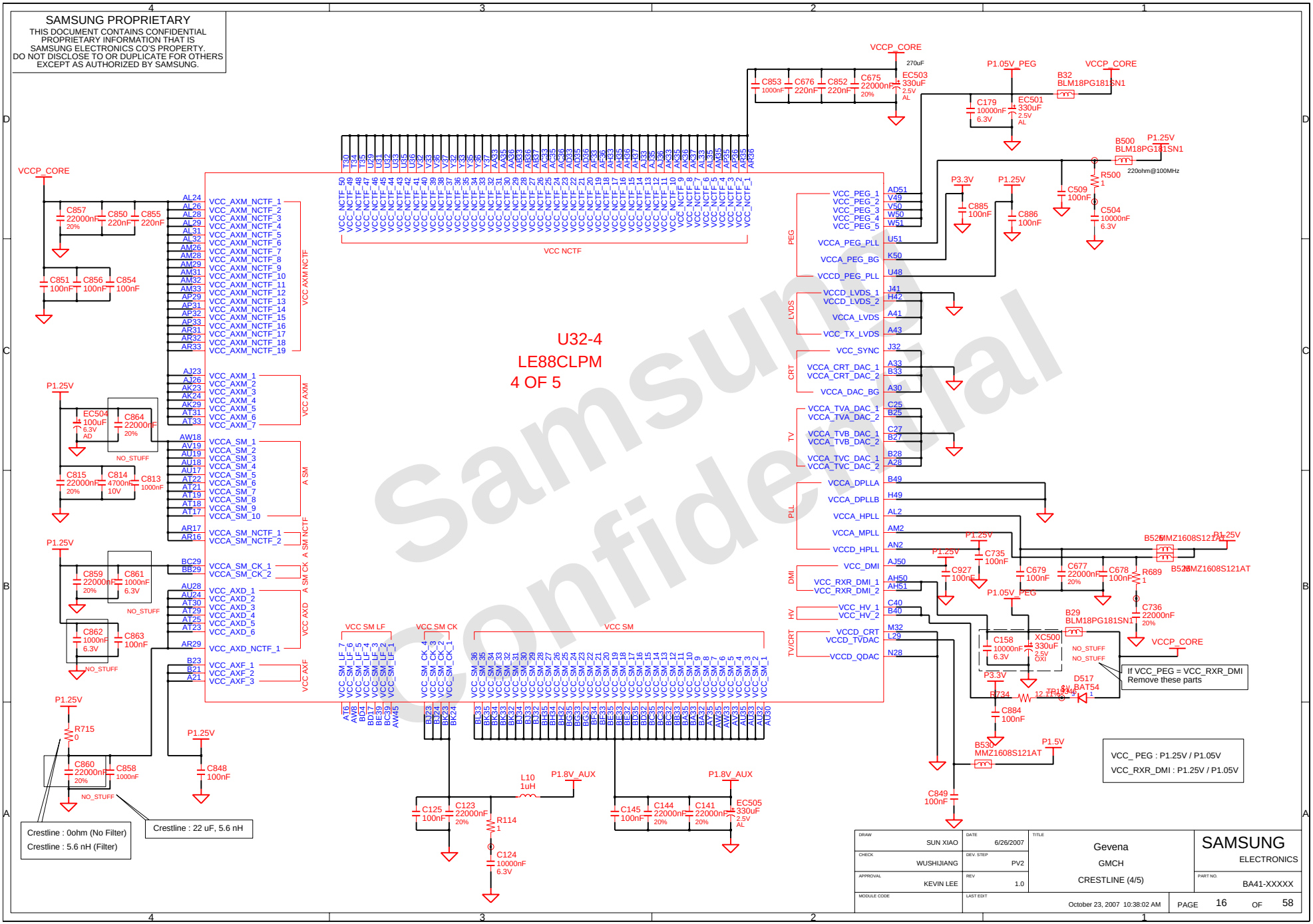
DRAW: SUN XIAO	DATE: 6/26/2007	TITLE: Gevena CMCH CRESTLINE (1/5)	SAMSUNG ELECTRONICS
CHECK: WUSHIJIANG	DEV. STEP: PV2		PART NO.: BA41-XXXXX
APPROVAL: KEVIN LEE	REV: 1.0		
MODULE CODE:	LAST EDIT: October 23, 2007 10:38:02 AM	PAGE 13 OF 58	



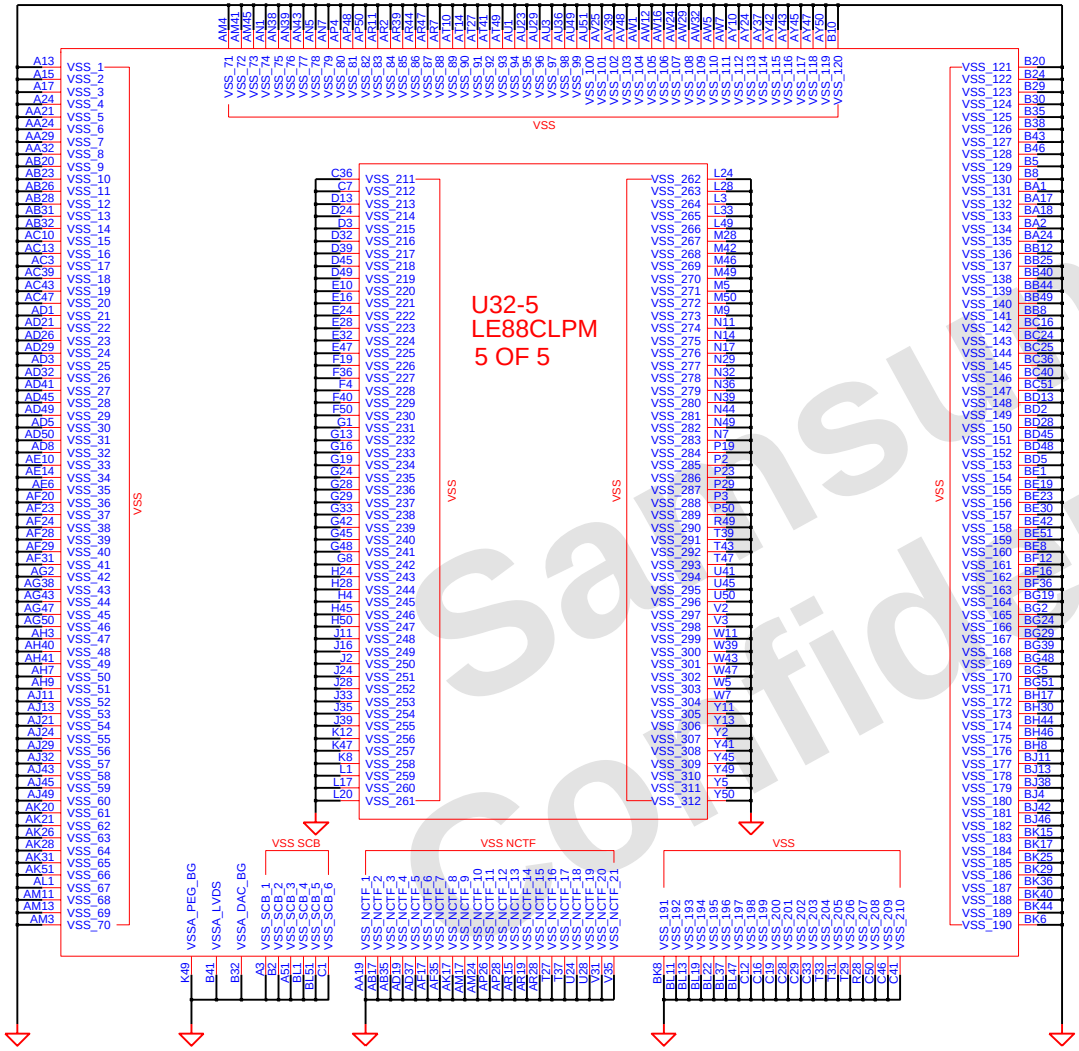
DRAW: SUN XIAO	DATE: 6/26/2007	TITLE: Gevena GMCH CRESTLINE (2/5)	SAMSUNG ELECTRONICS
CHECK: WUSHIJIANG	DEV. STEP: PV2		PART NO.: BA41-XXXXX
APPROVAL: KEVIN LEE	REV: 1.0		
MODULE CODE:	LAST EDIT: October 23, 2007 10:38:02 AM	PAGE 14 OF 58	



DRAW: SUN XIAO	DATE: 6/26/2007	TITLE: Gevena GMCH CRESTLINE (3/5)	SAMSUNG ELECTRONICS
CHECK: WUSHIJIANG	DEV. STEP: PV2		
APPROVAL: KEVIN LEE	REV: 1.0		PART NO.: BA41-XXXXX
MODULE CODE:	LAST EDIT: October 23, 2007 10:38:02 AM	PAGE 15 OF 58	



DRAW: SUN XIAO	DATE: 6/26/2007	TITLE: Gevena GMCH CRESTLINE (4/5)	SAMSUNG ELECTRONICS
CHECK: WUSHIJIANG	DEV. STEP: PV2		PART NO.: BA41-XXXXX
APPROVAL: KEVIN LEE	REV: 1.0		
MODULE CODE	LAST EDIT: October 23, 2007 10:38:02 AM	PAGE 16 OF 58	



*POCAFEB-11 Only (Remove in MP Model)

Current Setting (def. : default Option)		
CFG#	Low	High
CFG(5)	DMIx2	DMIx4 (def.)
CFG(6)	Reserved	DDR-II (def.)
CFG(7)	DT/Transportable	Mobile CPU (def.)
CFG(9)	PEG Reversal	Normal
CFG(16)	Dynamic ODT Disabled	Dynamic ODT Enabled (def.)
CFG(18)	VCC 1.05V (def.)	VCC 1.5V
CFG(19)	DMI Lane Normal	DMI Lane Reversal
CFG(20)	SDVO or PCIE X1 Only(def.)	SDVO and PCIE X1 Simultaneously

DRAW: SUN XIAO	DATE: 6/26/2007	TITLE: Gevena GMCH CRESTLINE (5/5)	SAMSUNG ELECTRONICS
CHECK: WUSHIJIANG	DEV. STEP: PV2		
APPROVAL: KEVIN LEE	REV: 1.0		PART NO.: BA41-XXXXX
MODULE CODE	LAST EDIT: October 23, 2007 10:38:02 AM	PAGE 17 OF 58	

Array resistors & Single resistors used to improve layout & routing.

ME POWER RAIL UNDER ME ENABLE

DDR1-1
DDR2-SODIMM-200P-RVS
1/2

DDR1-2
DDR2-SODIMM-200P-RVS
2/2

ME POWER RAIL UNDER ME ENABLE

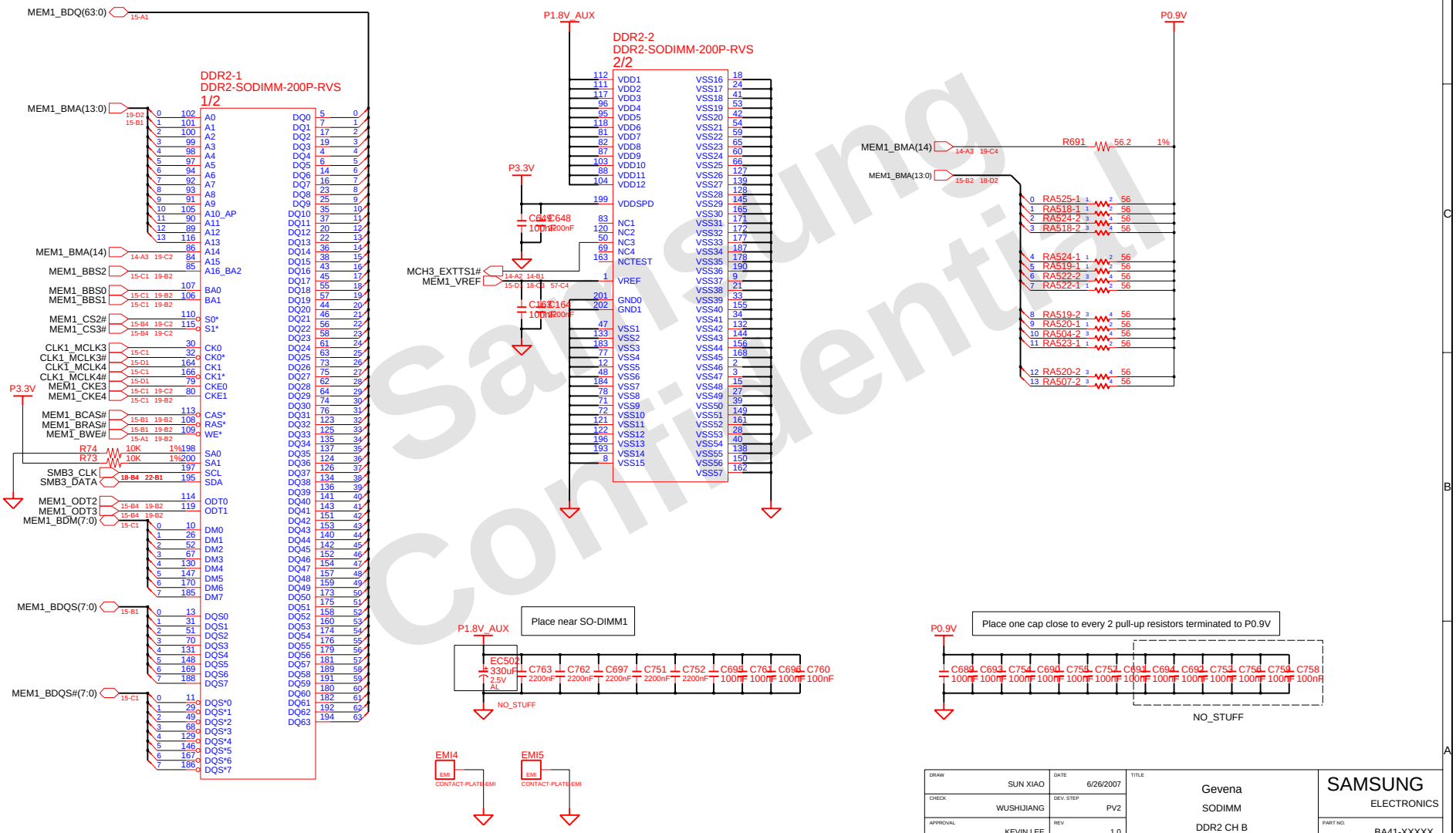
Place near SO-DIMM0

Place one cap close to every 2 pull-up resistors terminated to P0.9V

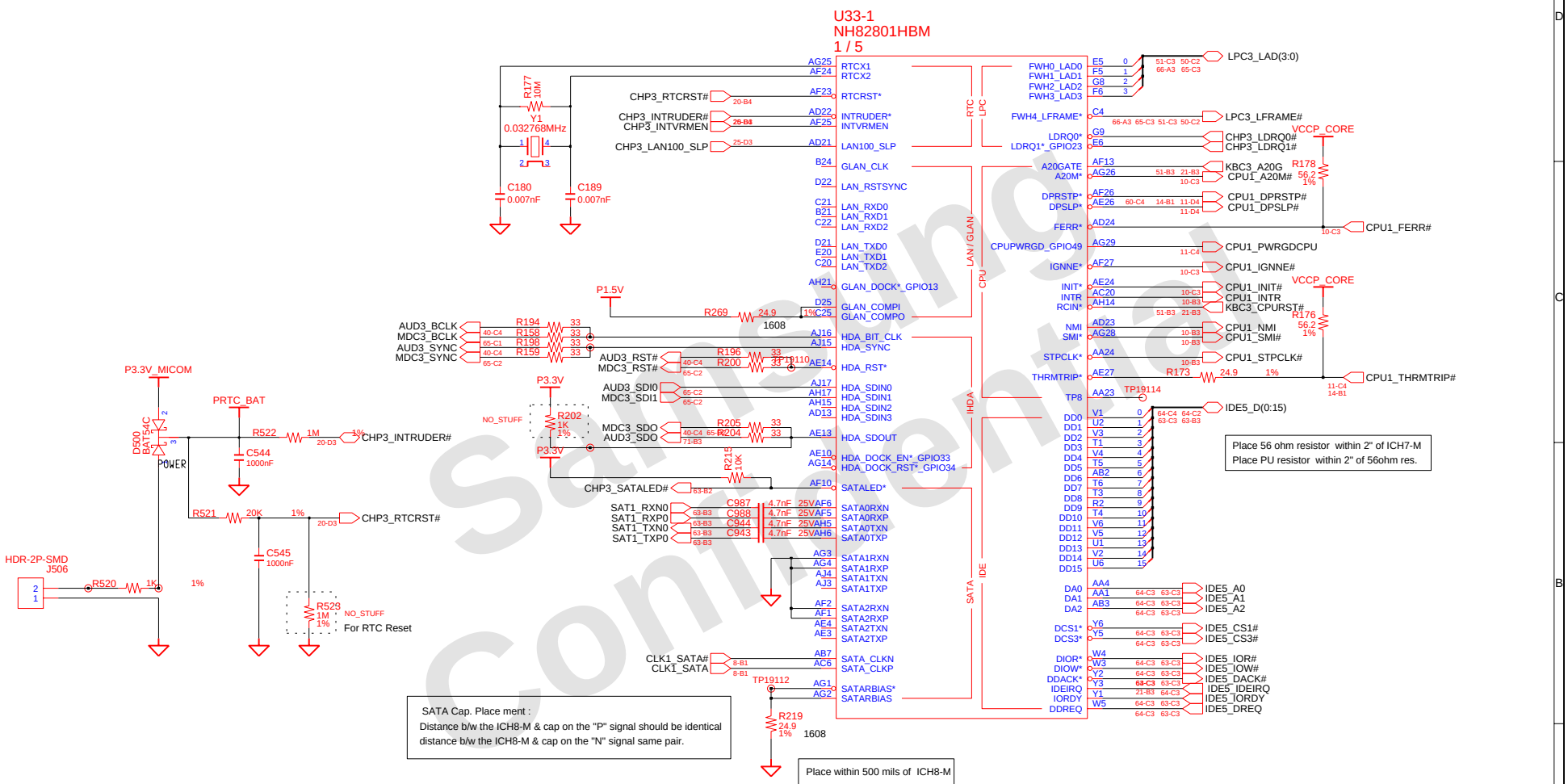
NO_STUFF

DRAW: SUN XIAO	DATE: 6/26/2007	TITLE: Gevena SODIMM DDR2 CH A	SAMSUNG ELECTRONICS
CHECK: WUSHIJIANG	DEV. STEP: PV2		
APPROVAL: KEVIN LEE	REV: 1.0		PART NO.: BA41-XXXXX
MODULE CODE:	LAST EDIT: October 23, 2007 10:38:02 AM	PAGE 18 OF 58	

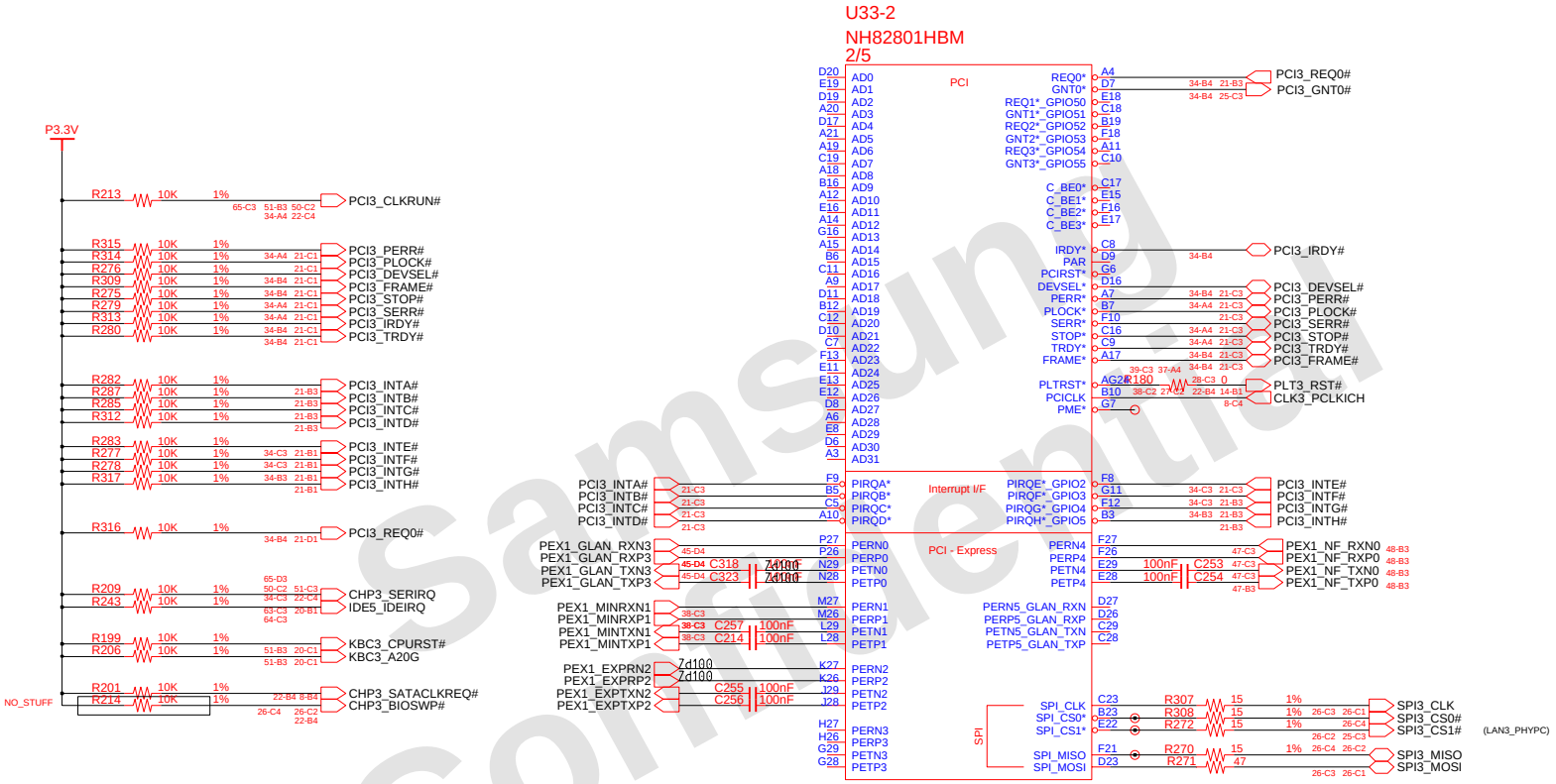
DDR SO-DIMM #1



DRAW: SUN XIAO	DATE: 6/26/2007	TITLE: Gevena SODIMM DDR2 CH B	SAMSUNG ELECTRONICS
CHECK: WUSHIJIANG	DEV. STEP: PV2		
APPROVAL: KEVIN LEE	REV: 1.0		PART NO.: BA41-XXXXX
MODULE CODE	LAST EDIT: October 23, 2007 10:38:02 AM	PAGE 19 OF 58	



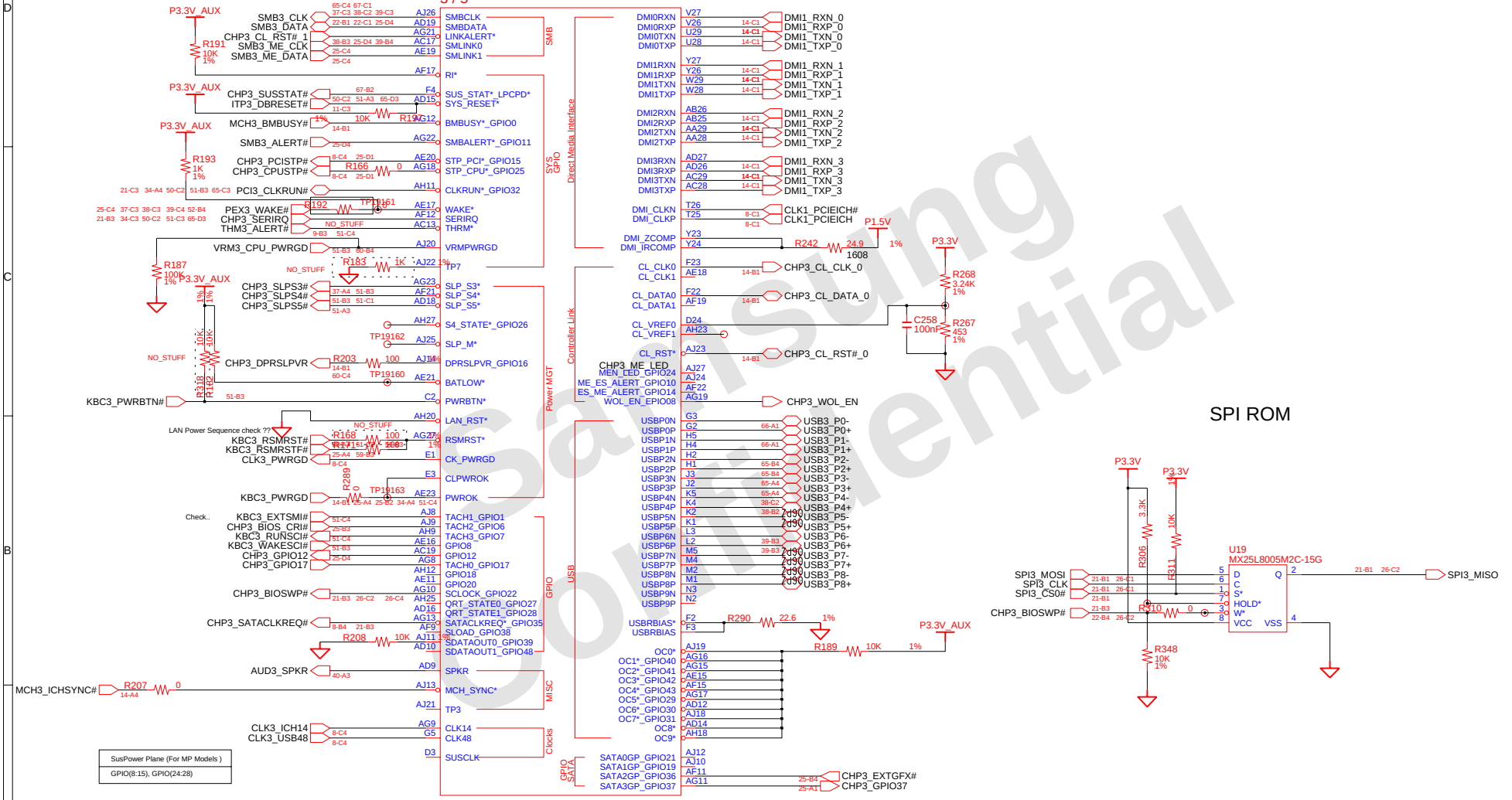
DRAW: SUN XIAO	DATE: 6/26/2007	TITLE: Gevena ICH8-M ICH8-M (1/5)	SAMSUNG ELECTRONICS
CHECK: WUSHIJIANG	DEV. STEP: PV2		
APPROVAL: KEVIN LEE	REV: 1.0		PART NO.: BA41-XXXXX
MODULE CODE:	LAST EDIT: October 23, 2007 10:38:02 AM	PAGE 20 OF 58	



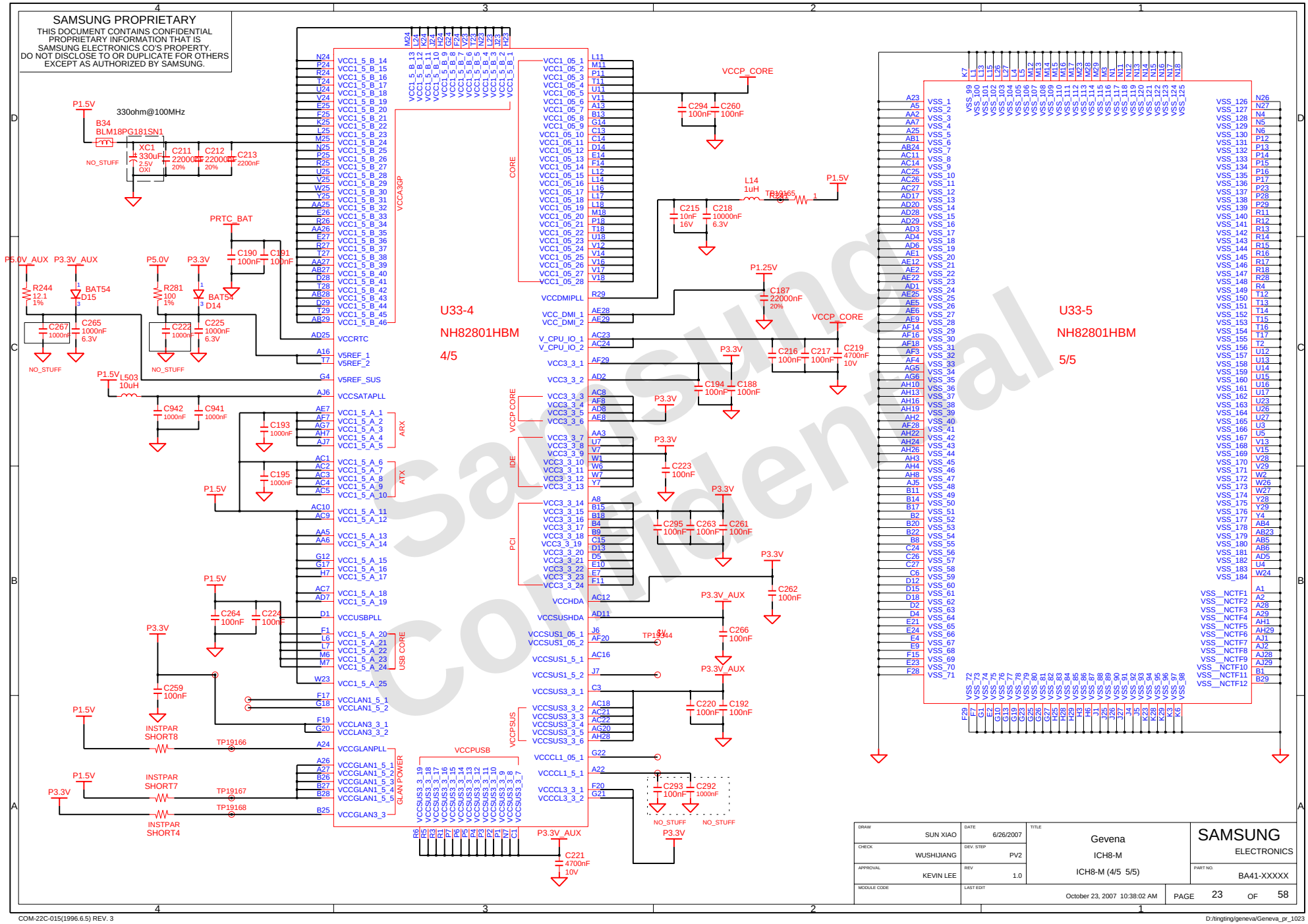
AC caps : PCIE need to be within 250mils of the driver
Resistor for Test : Place Stuffing Option to minimize stubs

DRAW: SUN XIAO	DATE: 6/26/2007	TITLE: Gevena ICH8-M ICH8-M (2/5)	SAMSUNG ELECTRONICS
CHECK: WUSHIJIANG	DEV. STEP: PV2		
APPROVAL: KEVIN LEE	REV: 1.0		PART NO.: BA41-XXXXX
MODULE CODE:	LAST EDIT: October 23, 2007 10:38:02 AM	PAGE 21 OF 58	

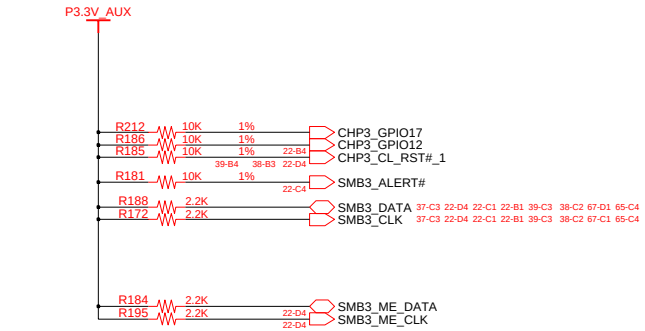
U33-3 NH82801HBM 3 / 5

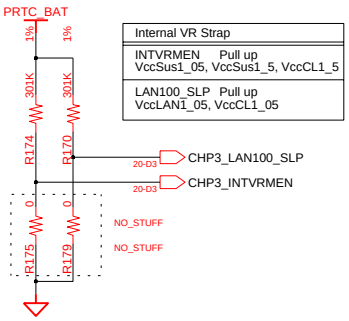


DRAW: SUN XIAO	DATE: 6/26/2007	TITLE: Gevena ICH8-M ICH8-M (3/5)	SAMSUNG ELECTRONICS
CHECK: WUSHIJIANG	DEV. STEP: PV2		
APPROVAL: KEVIN LEE	REV: 1.0		PART NO.: BA41-XXXXX
MODULE CODE	LAST EDIT: October 23, 2007 10:38:02 AM	PAGE 22 OF 58	



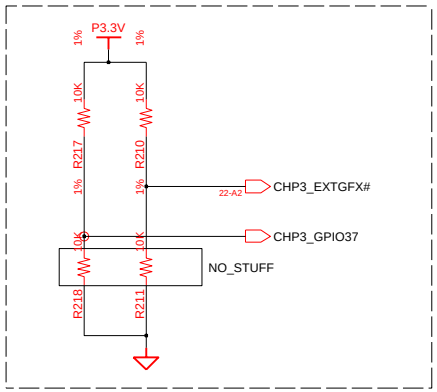
DRAW: SUN XIAO	DATE: 6/26/2007	TITLE: Gevena ICH8-M ICH8-M (4/5 5/5)	SAMSUNG ELECTRONICS
CHECK: WUSHIJIANG	DEV. STEP: PV2		
APPROVAL: KEVIN LEE	REV: 1.0		PART NO.: BA41-XXXXX
MODULE CODE:	LAST EDIT: October 23, 2007 10:38:02 AM	PAGE 23 OF 58	

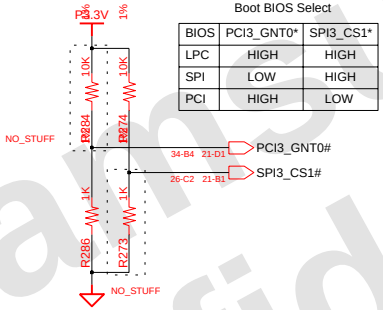




Internal VR Strap
INTVRMEN Pull up VccSus1_05, VccSus1_5, VccCL1_5
LAN100_SLP Pull up VccLAN1_05, VccCL1_05

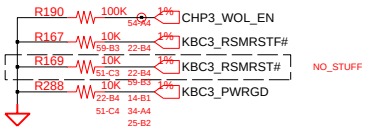
Model Dependent

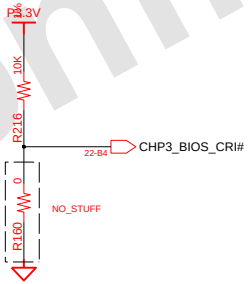




Boot BIOS Select

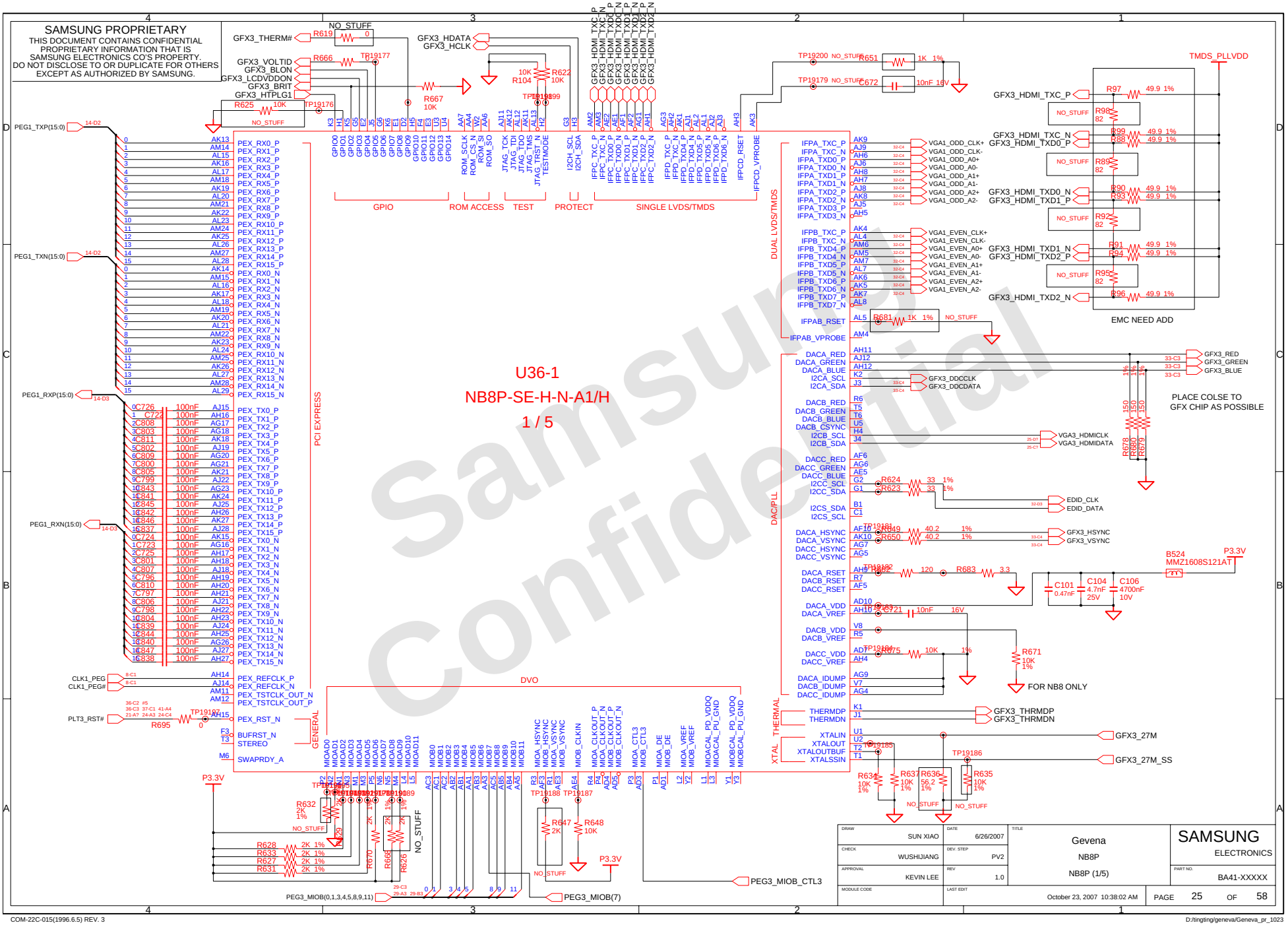
BIOS	PCI3_GNT0*	SPI3_CS1*
LPC	HIGH	HIGH
SPI	LOW	HIGH
PCI	HIGH	LOW



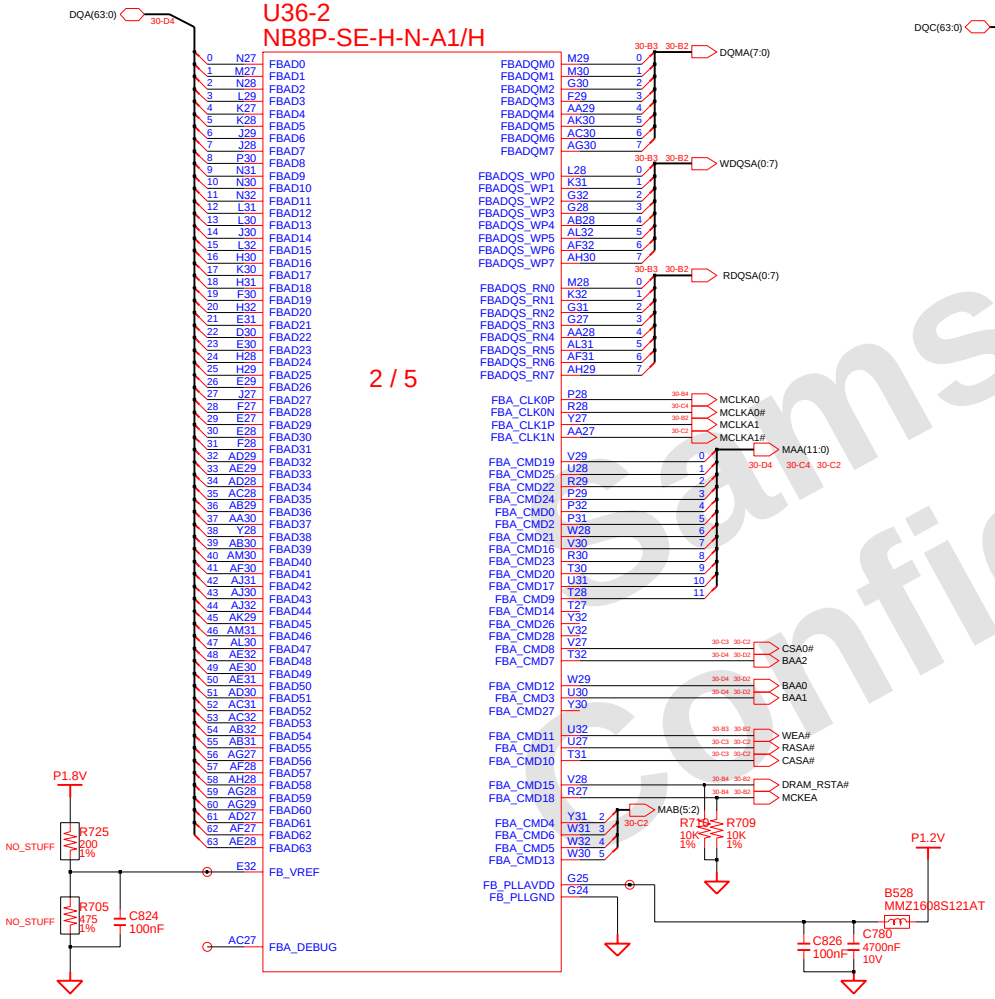


BIOS CRISIS RECOVER STRAP
PLACE NEAR KEYBOARD

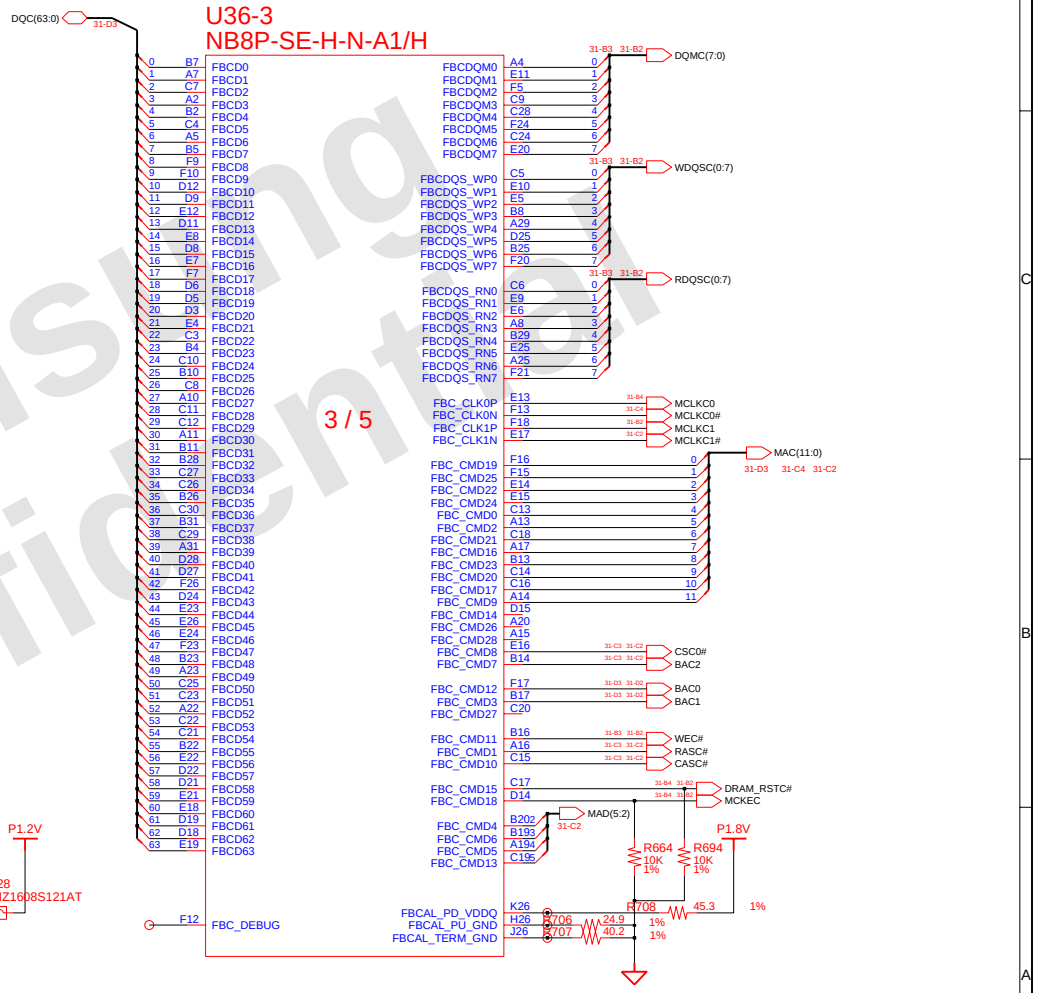
DRAW: SUN XIAO	DATE: 6/26/2007	TITLE: Gevena / ICH8-M / ICH8-M STAP	SAMSUNG ELECTRONICS
CHECK: WUSHIJIANG	DEV. STEP: PV2		
APPROVAL: KEVIN LEE	REV: 1.0		PART NO.: BA41-XXXXX
MODULE CODE	LAST EDIT: October 23, 2007 10:38:02 AM	PAGE 24 OF 58	



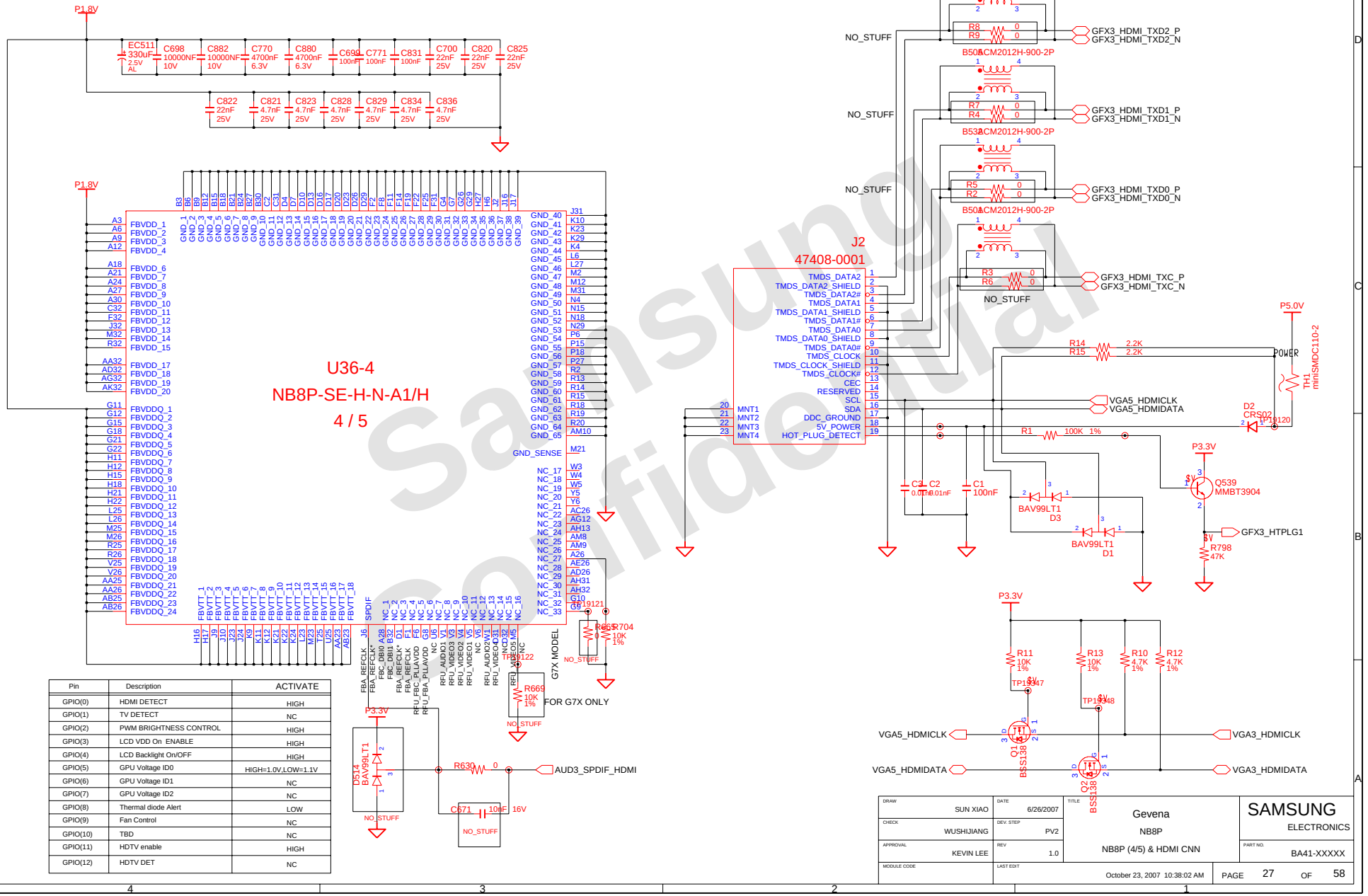
Graphic Memory I/F (Using FBA Channel)



Graphic Memory I/F (Using FBC Channel)

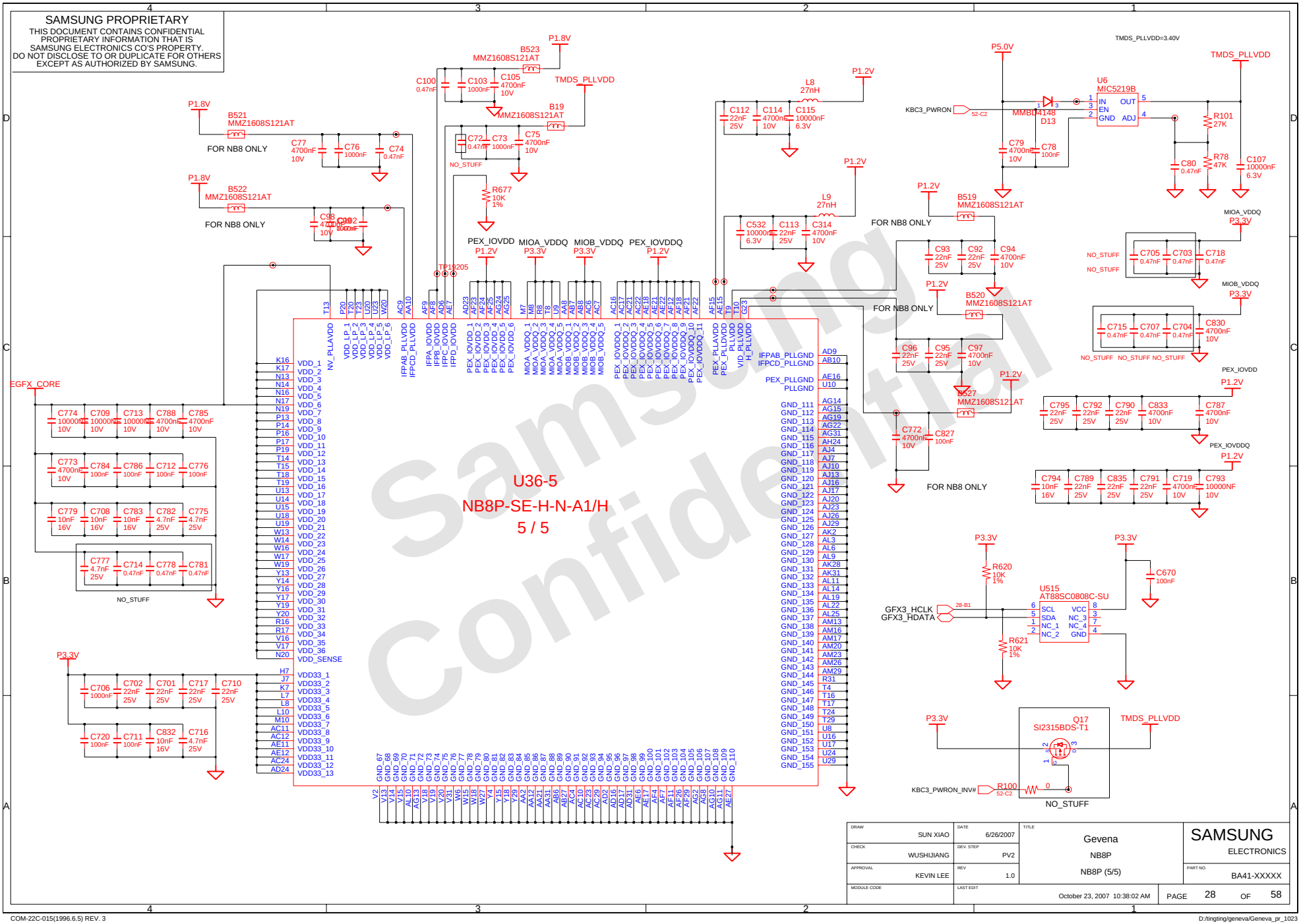


DRAW: SUN XIAO	DATE: 6/26/2007	TITLE: Gevena NB8P NB8P (2/5 3/5)	SAMSUNG ELECTRONICS
CHECK: WUSHIJIANG	DEV. STEP: PV2		
APPROVAL: KEVIN LEE	REV: 1.0		PART NO.: BA41-XXXXX
MODULE CODE	LAST EDIT: October 23, 2007 10:38:02 AM	PAGE 26 OF 58	



Pin	Description	ACTIVATE
GPIO(0)	HDMI DETECT	HIGH
GPIO(1)	TV DETECT	NC
GPIO(2)	PWM BRIGHTNESS CONTROL	HIGH
GPIO(3)	LCD VDD On ENABLE	HIGH
GPIO(4)	LCD Backlight On/OFF	HIGH
GPIO(5)	GPU Voltage ID0	HIGH=1.0V,LOW=1.1V
GPIO(6)	GPU Voltage ID1	NC
GPIO(7)	GPU Voltage ID2	NC
GPIO(8)	Thermal diode Alert	LOW
GPIO(9)	Fan Control	NC
GPIO(10)	TBD	NC
GPIO(11)	HDTV enable	HIGH
GPIO(12)	HDTV DET	NC

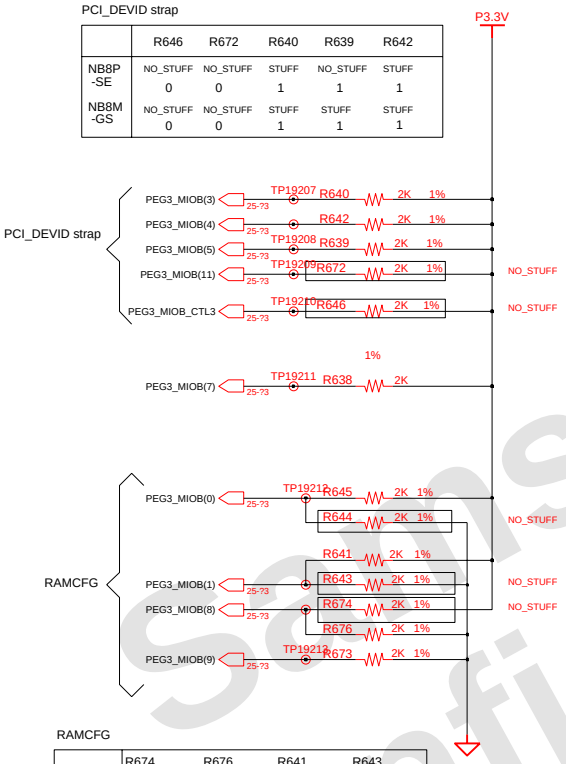
DRAW: SUN XIAO	DATE: 6/26/2007	TITLE: Gevena NB8P NB8P (4/5) & HDMI CNN	SAMSUNG ELECTRONICS
CHECK: WUSHIJIANG	DEV. STEP: PV2		
APPROVAL: KEVIN LEE	REV: 1.0		PART NO.: BA41-XXXXX
MODULE CODE	LAST EDIT: October 23, 2007 10:38:02 AM	PAGE 27 OF 58	



DRAW: SUN XIAO	DATE: 6/26/2007	TITLE: Gevena NB8P NB8P (5/5)	SAMSUNG ELECTRONICS
CHECK: WUSHIJIANG	DEV. STEP: PV2		
APPROVAL: KEVIN LEE	REV: 1.0		PART NO.: BA41-XXXXX
MODULE CODE	LAST EDIT: October 23, 2007 10:38:02 AM	PAGE 28 OF 58	

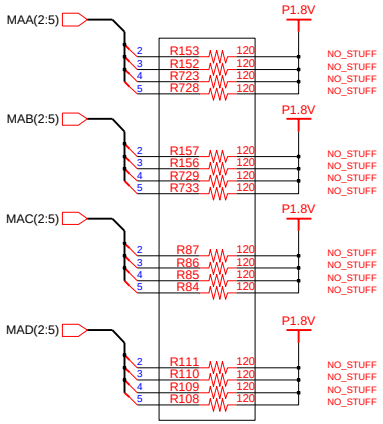
PCI_DEVID strap

	R646	R672	R640	R639	R642
NB8P-SE	NO_STUFF	NO_STUFF	STUFF	NO_STUFF	STUFF
	0	0	1	1	1
NB8M-GS	NO_STUFF	NO_STUFF	STUFF	STUFF	STUFF
	0	0	1	1	1



Straps		Pin # (Rev.A02)	Descriptions
SUB_VENDOR		MIOAD(1)	0 : No BIOS 1 : Read from BIOS
RAMCFG(3:0) [9,8,1,0]		MIOB(9) MIOB(8) MIOB(1) MIOB(0)	0111 : SAMSUNG GDDR3 256Mbit 0101 : INFINEON GDDR3 256Mbit 0011 : SAMSUNG GDDR3 512Mbit 0001 : INFINEON GDDR3 512Mbit
CRYSTAL(1:0)		MIOB(2) MIOB(6)	01 : 14.318 MHz 10 : 27 MHz 11 : Unknown 00 : 13.5 MHz
TV_MODE(1:0)		MIOAD(7) MIOAD(10)	00 : SECAM 01 : NTSC 10 : PAL 11 : CRT
PCI_DEVID(4:0) [CTL3,11,3,5,4]		MIOB_CTL(3) MIOB(11) MIOB(3) MIOB(5) MIOB(4)	NB8M-GS: 00111 NB8M-SE: 01000 NB8M-GT: 00110 NB8P-GS: 00111 NB8P-SE: 00101 NB8P-GT: 01000
ROM_TYPE(1:0)		MIOB(10) MIOBVSYNC	NO ROM(NC)
USER STRAP		MIOAD(2:5)	EDID
GPIO(12:0)		Sheet 25	Refer to Sheet 25

Test Options for GPIO should be updated..



RAMCFG

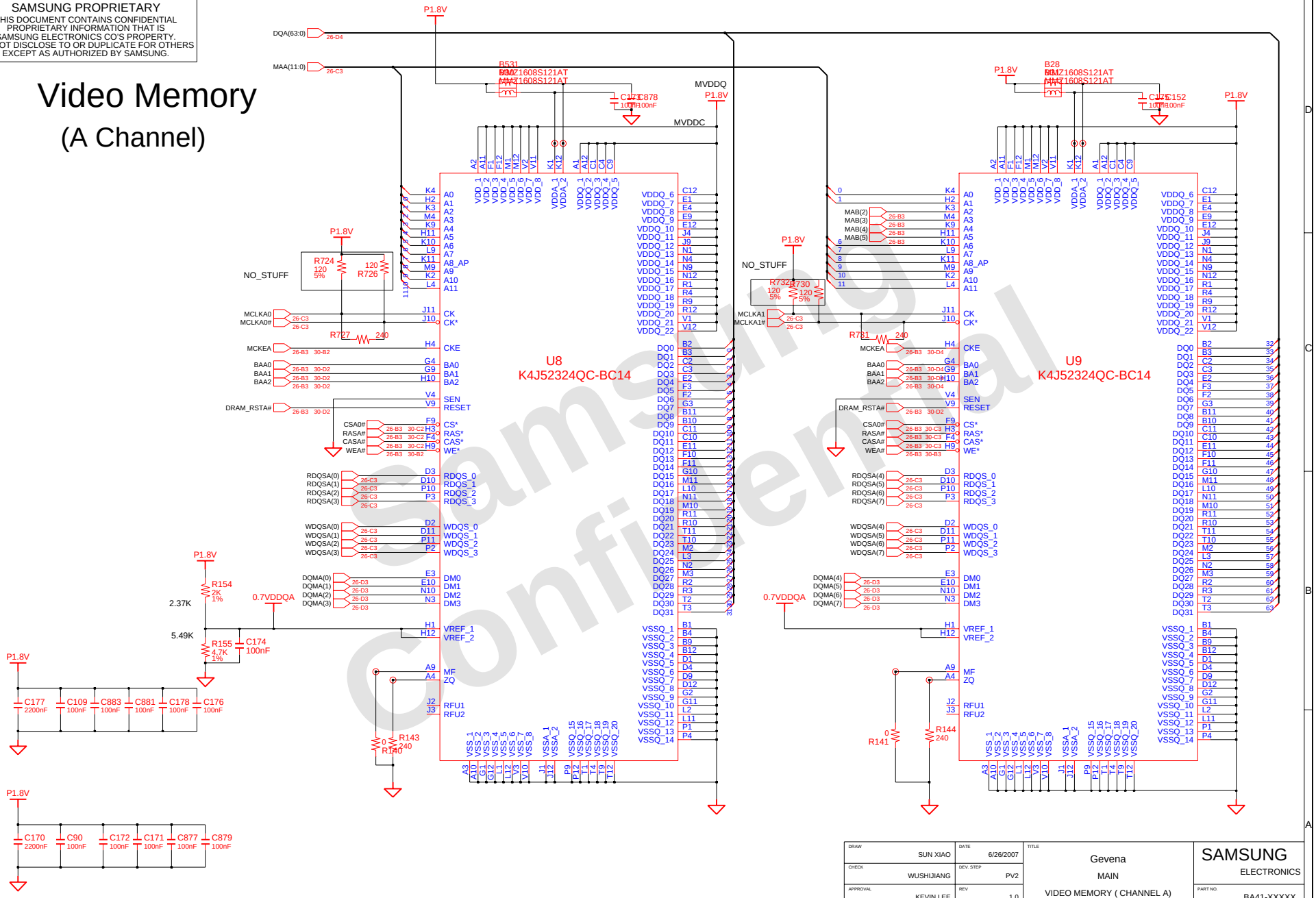
	R674	R676	R641	R643
SS 256Mbit	STUFF	NO_STUFF	STUFF	NO_STUFF
IF 256Mbit	STUFF	NO_STUFF	NO_STUFF	STUFF
SS 512Mbit	NO_STUFF	STUFF	STUFF	NO_STUFF
IF 512Mbit	NO_STUFF	STUFF	NO_STUFF	STUFF

Samsung		Infineon	
256Mbit	512Mbit	256Mbit	512Mbit
K4J55323QG (1.2/1.4/1.6/2.0) K4J55323QF (1.4/1.6/2.0)	K4J52324QC (1.2/1.4/1.6/2.0)	HYB18H256321AFL20(2.0) HYB18H256321AFL16(1.6) HYB18H256324AF-20(2.0) HYB18H256321AF-14(1.4) HYB18H256321AF-12(1.2)	HYB18H512321AFL20(2.0) HYB18H512321AFL16(1.6) HYB18H512324AF-20(1.6) HYB18H512321AF-14(1.4) HYB18H512321AF-12(1.2)
8M*32BIT	16M*32BIT	8M*32BIT	16M*32BIT

DRAW: SUN XIAO	DATE: 6/26/2007	TITLE: Gevena NB8P NB8P STRAP	SAMSUNG ELECTRONICS
CHECK: WUSHIJIANG	DEV. STEP: PV2		
APPROVAL: KEVIN LEE	REV: 1.0		PART NO.: BA41-XXXXX
MODULE CODE	LAST EDIT: October 23, 2007 10:38:02 AM	PAGE 29 OF 58	

Video Memory

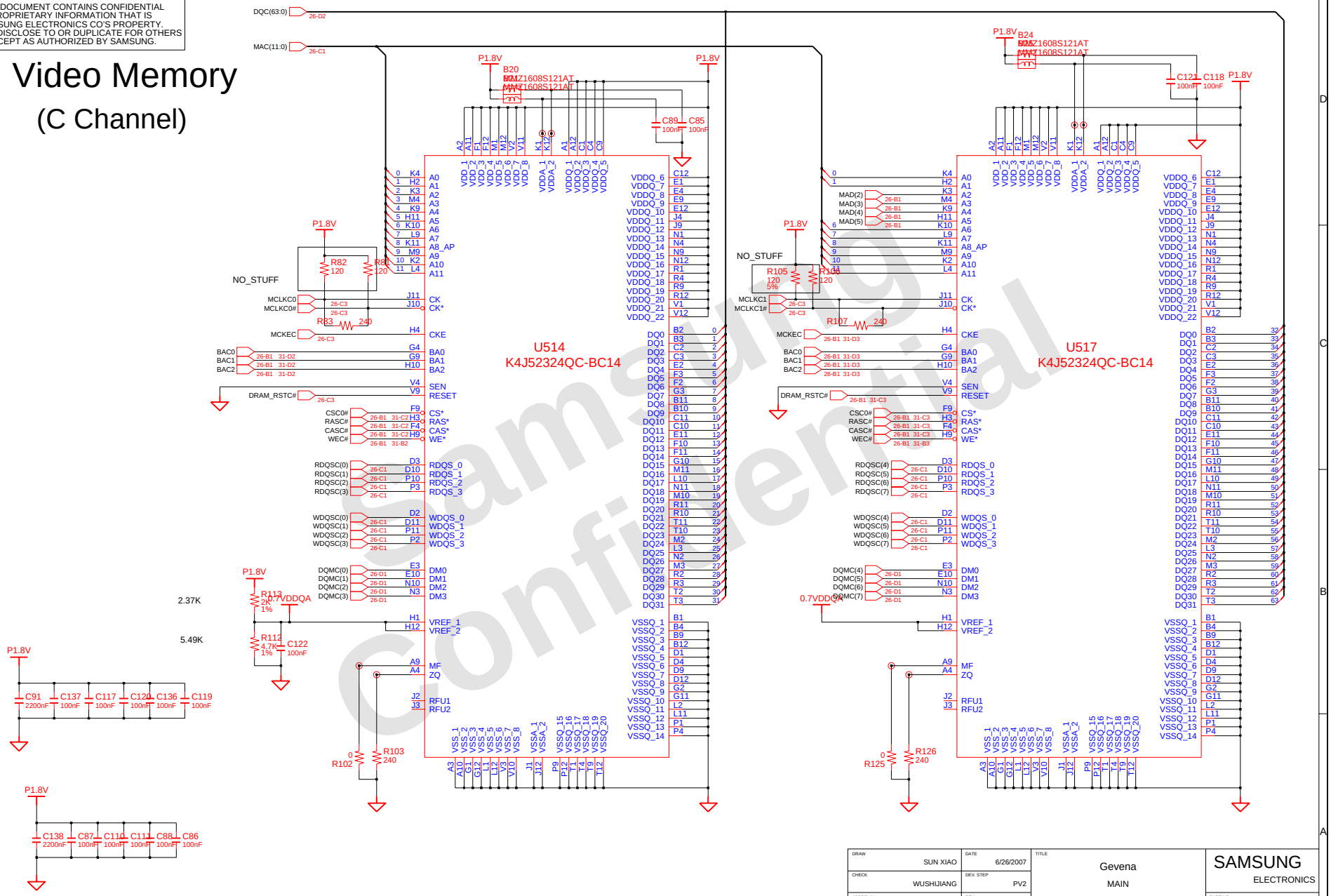
(A Channel)



DRAW: SUN XIAO	DATE: 6/26/2007	TITLE: Gevena / MAIN / VIDEO MEMORY (CHANNEL A)	SAMSUNG ELECTRONICS
CHECK: WUSHIJIANG	DEV. STEP: PV2		
APPROVAL: KEVIN LEE	REV: 1.0		PART NO.: BA41-XXXXX
MODULE CODE	LAST EDIT: October 23, 2007 10:38:02 AM	PAGE 30 OF 58	

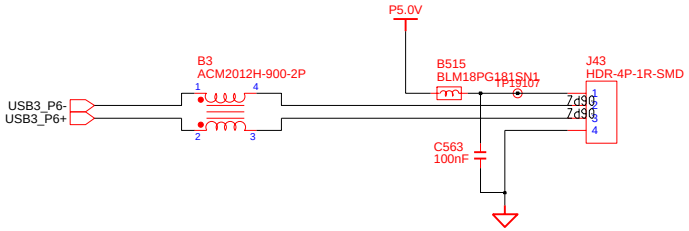
Video Memory

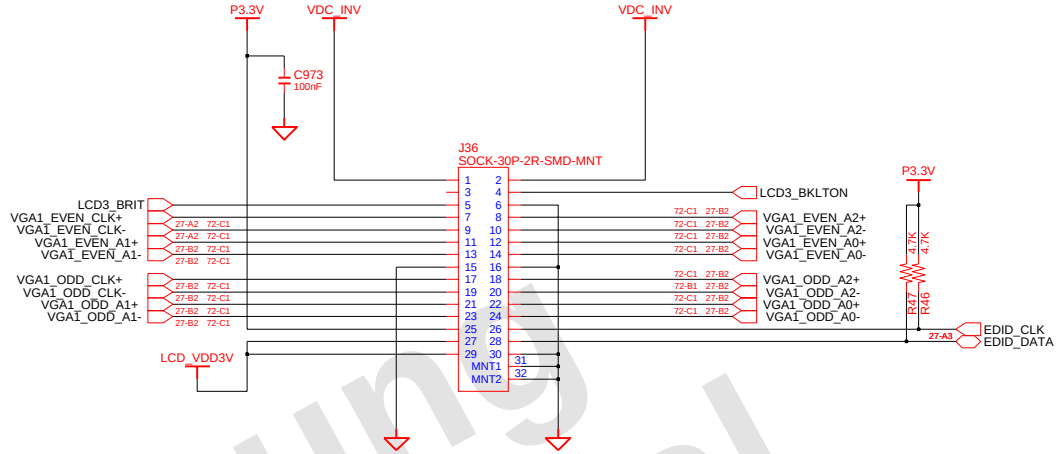
(C Channel)

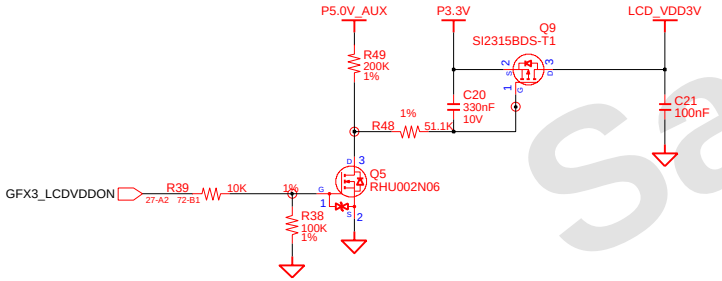


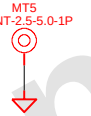
DRAW: SUN XIAO	DATE: 6/26/2007	TITLE: Gevena / MAIN / VIDEO MEMORY (CHANNEL B)	SAMSUNG ELECTRONICS
CHECK: WUSHIJIANG	DEV. STEP: PV2		
APPROVAL: KEVIN LEE	REV: 1.0		PART NO.: BA41-XXXXX
MODULE CODE:	LAST EDIT: October 23, 2007 10:38:02 AM	PAGE 31 OF 58	

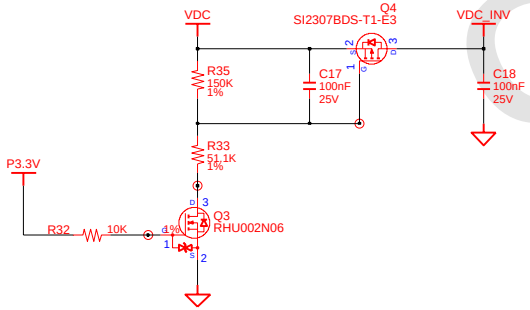
USB CAMERA FUNCTION

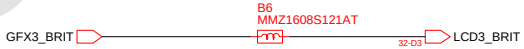


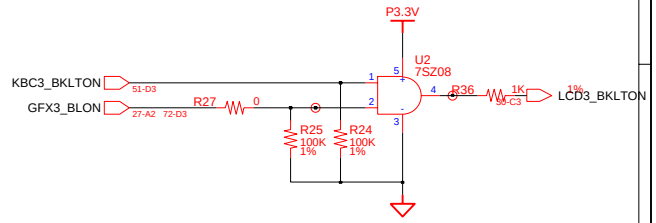






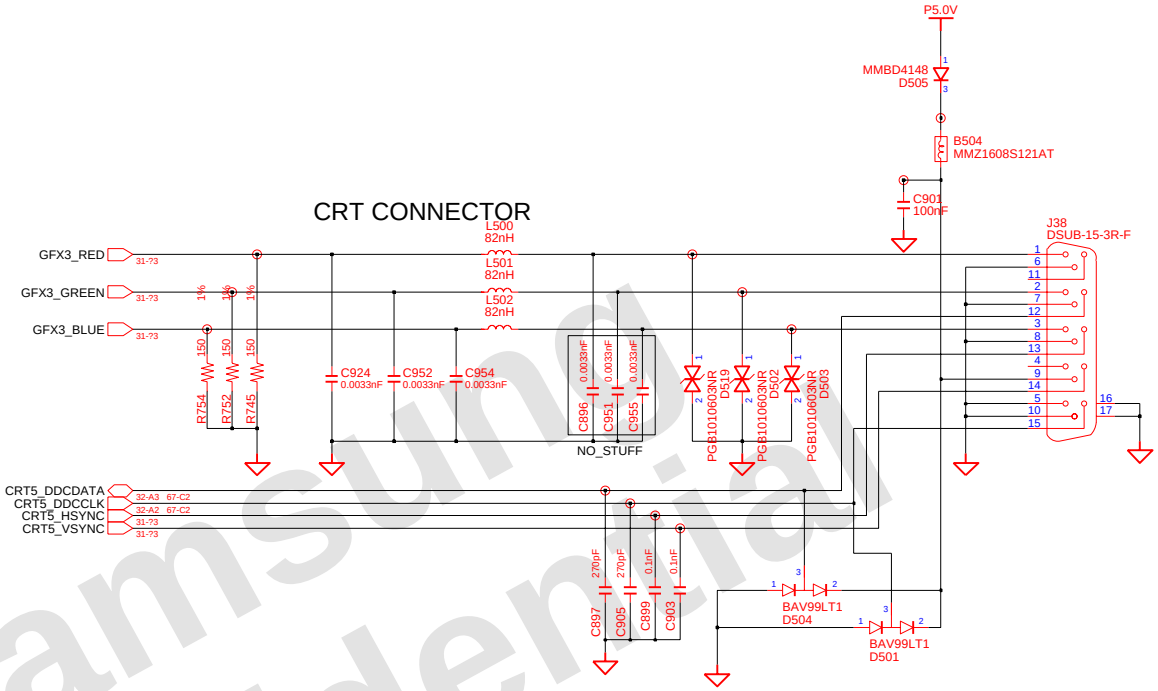


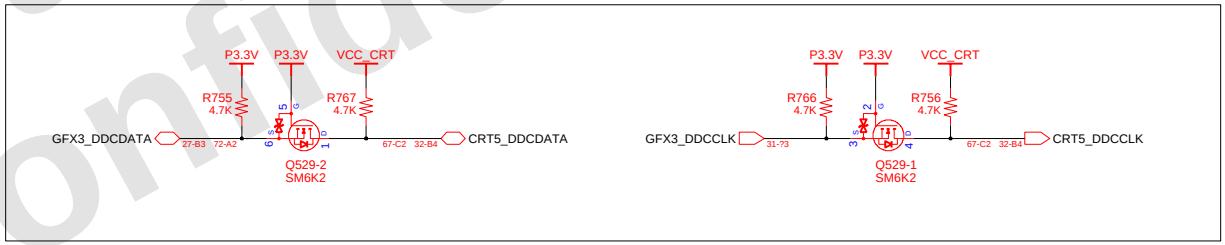


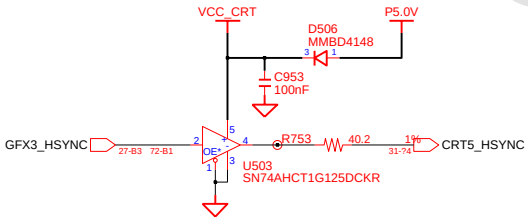


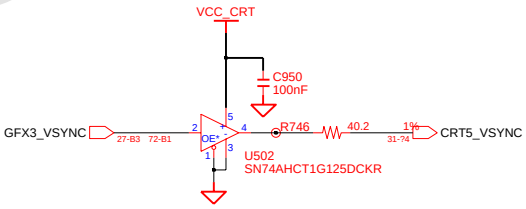
DRAW: SUN XIAO	DATE: 6/26/2007	TITLE: Gevena LCD CONNECTER & SPEAD SPECTRUM	SAMSUNG ELECTRONICS
CHECK: WUSHIJIANG	DEV. STEP: PV2		
APPROVAL: KEVIN LEE	REV: 1.0		PART NO.: BA41-XXXXX
MODULE CODE:	LAST EDIT: October 23, 2007 10:38:02 AM	PAGE 32 OF 58	

CRT CONNECTOR

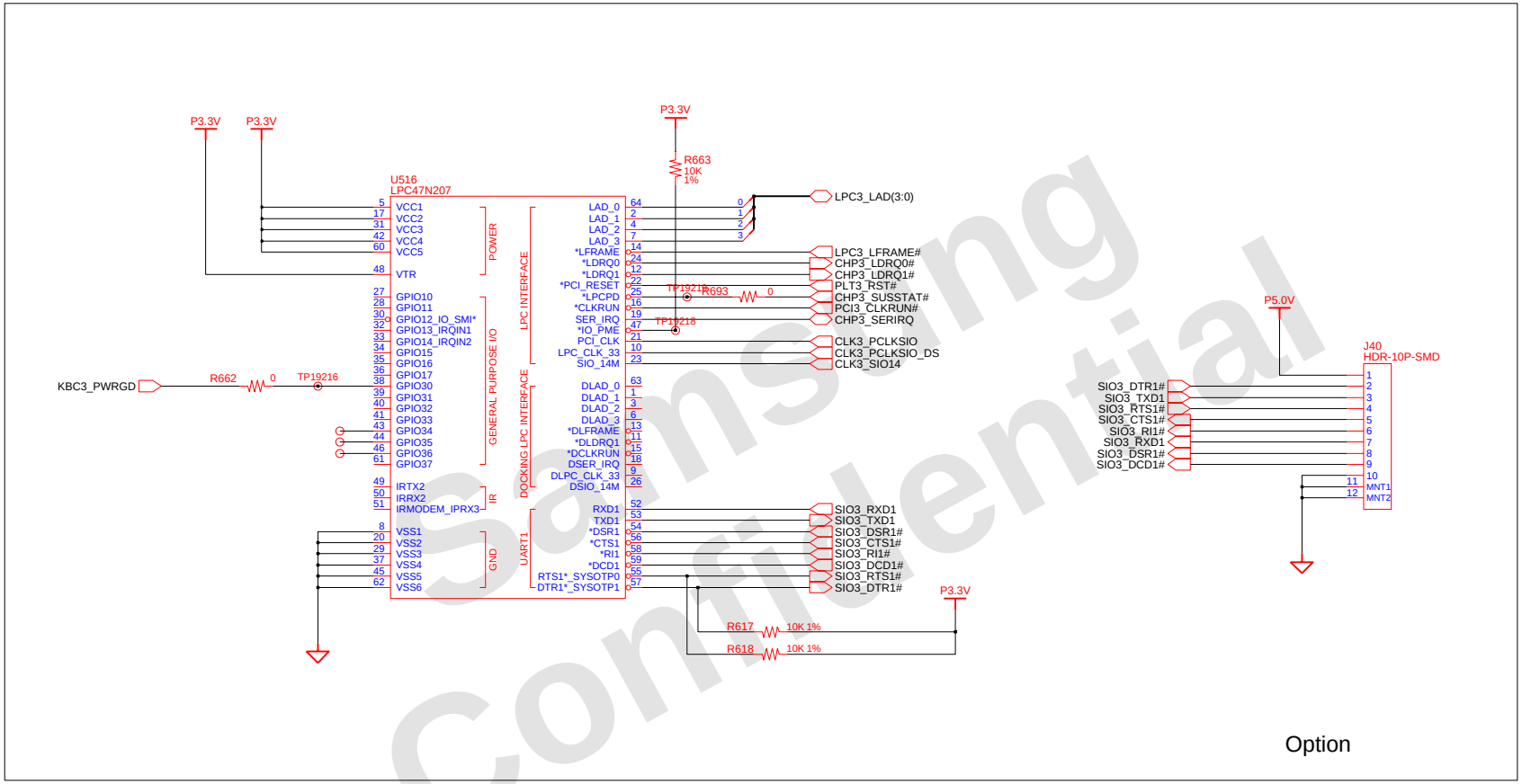




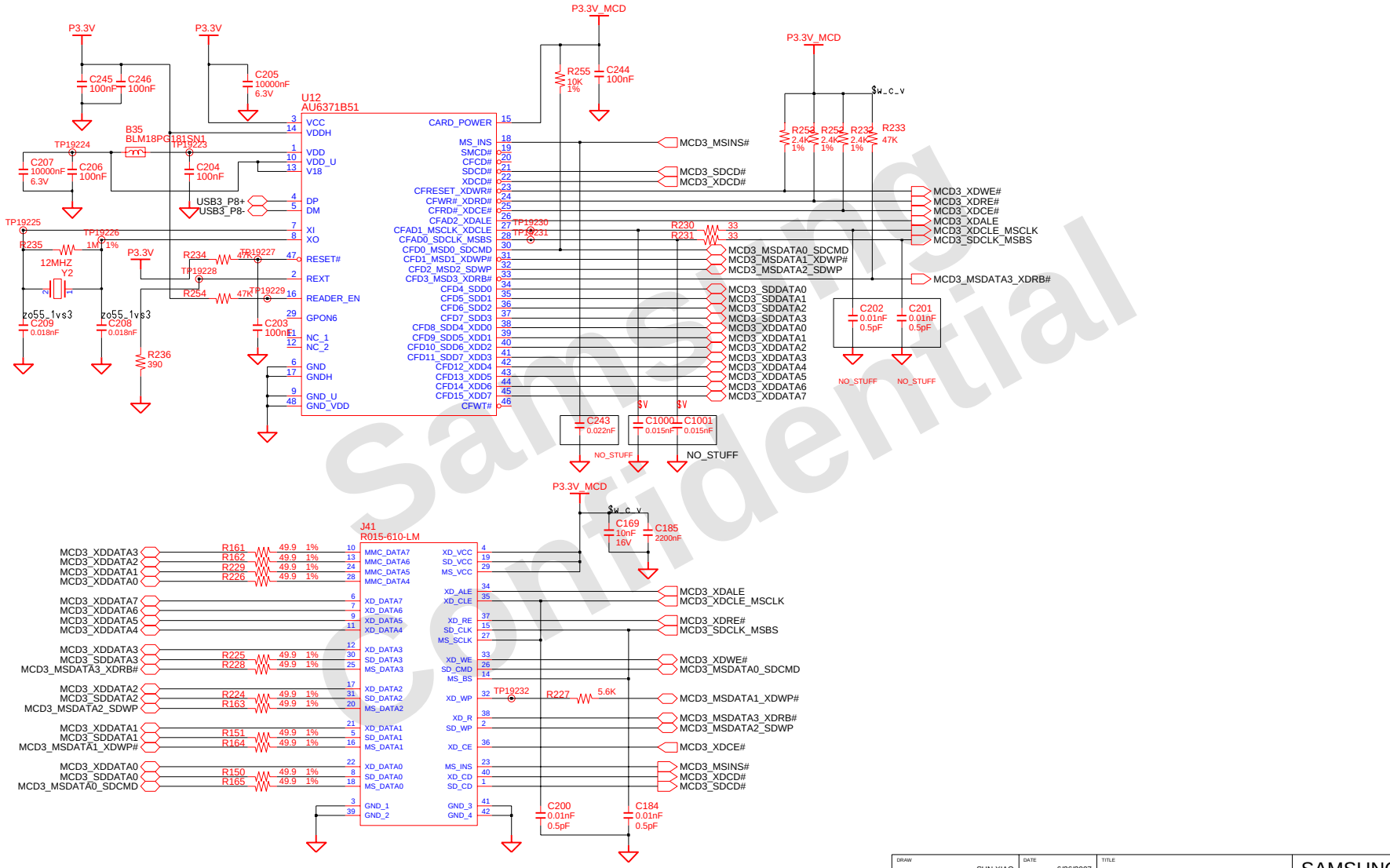




DRAW: SUN XIAO	DATE: 6/26/2007	TITLE: Gevena / MIAN / CRT PORT	SAMSUNG ELECTRONICS
CHECK: WUSHIJIANG	DEV. STEP: PV2		
APPROVAL: KEVIN LEE	REV: 1.0		PART NO.: BA41-XXXXX
MODULE CODE	LAST EDIT: October 23, 2007 10:38:02 AM	PAGE 33 OF 58	

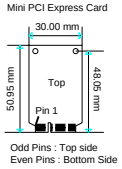


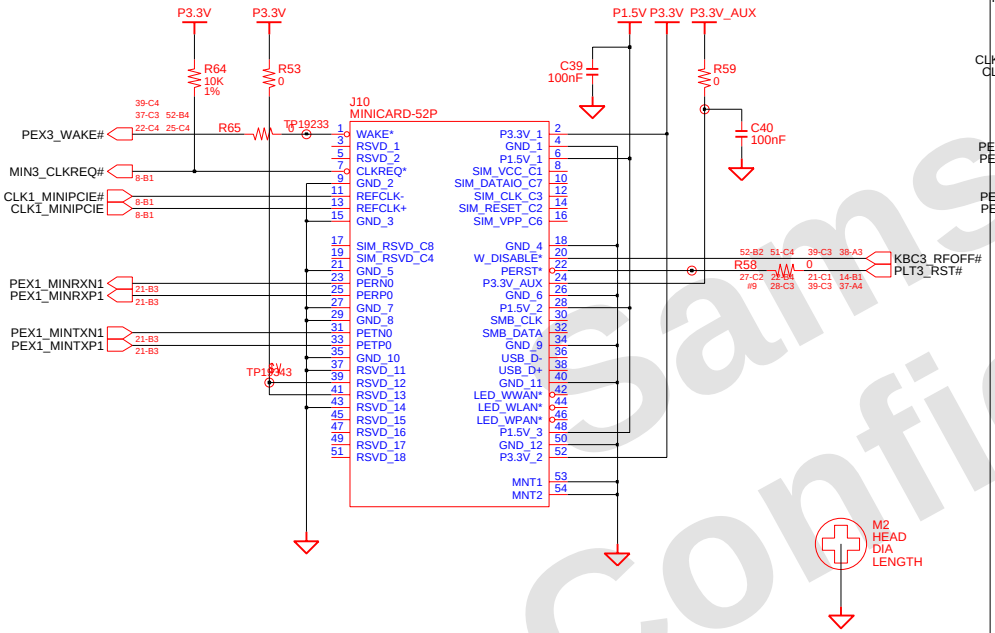
DRAW: SUN XIAO	DATE: 6/26/2007	TITLE: Gevena SIO CHIPSET	SAMSUNG ELECTRONICS
CHECK: WUSHIJIANG	DEV. STEP: PV2		
APPROVAL: KEVIN LEE	REV: 1.0		PART NO.: BA41-
MODULE CODE:	LAST EDIT: October 23, 2007 10:38:02 AM	PAGE 34 OF 69	

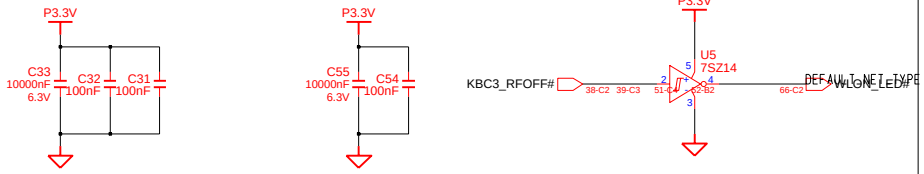


DRAW: SUN XIAO	DATE: 6/26/2007	TITLE: Gevena CARDREADER 7 IN 1	SAMSUNG ELECTRONICS
CHECK: WUSHIJIANG	DEV. STEP: PV2		
APPROVAL: KEVIN LEE	REV: 1.0		PART NO.: BA41-
MODULE CODE:	LAST EDIT: October 23, 2007 10:38:02 AM	PAGE 35 OF 68	

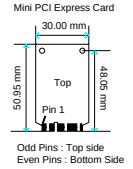
Mini Card

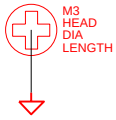


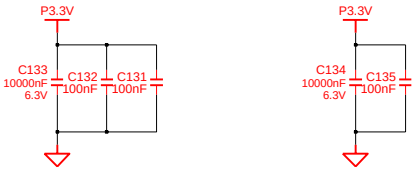




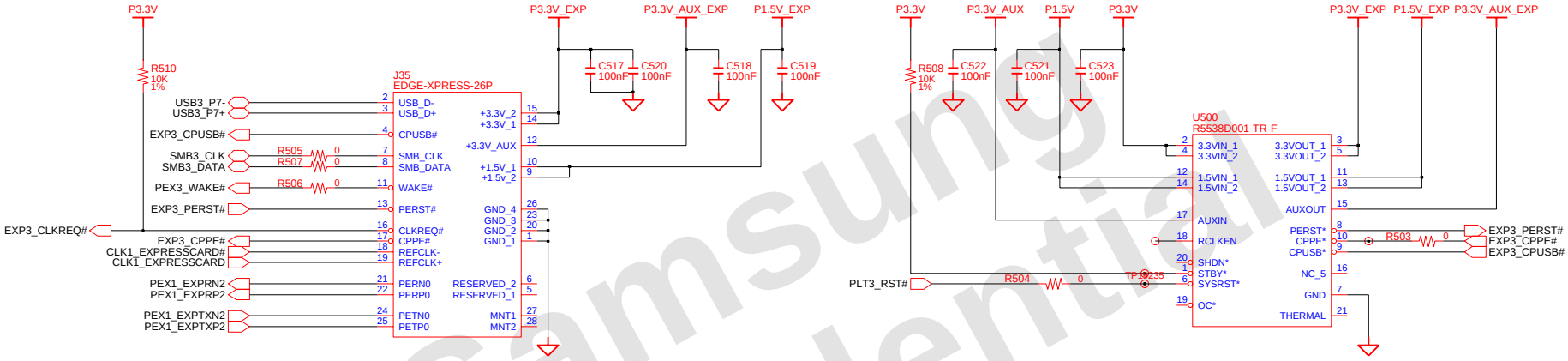
MINI CARD FOR ROBSON

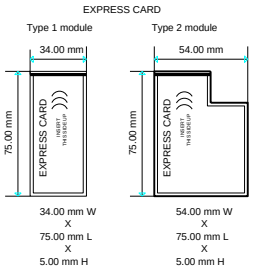


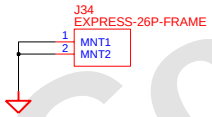




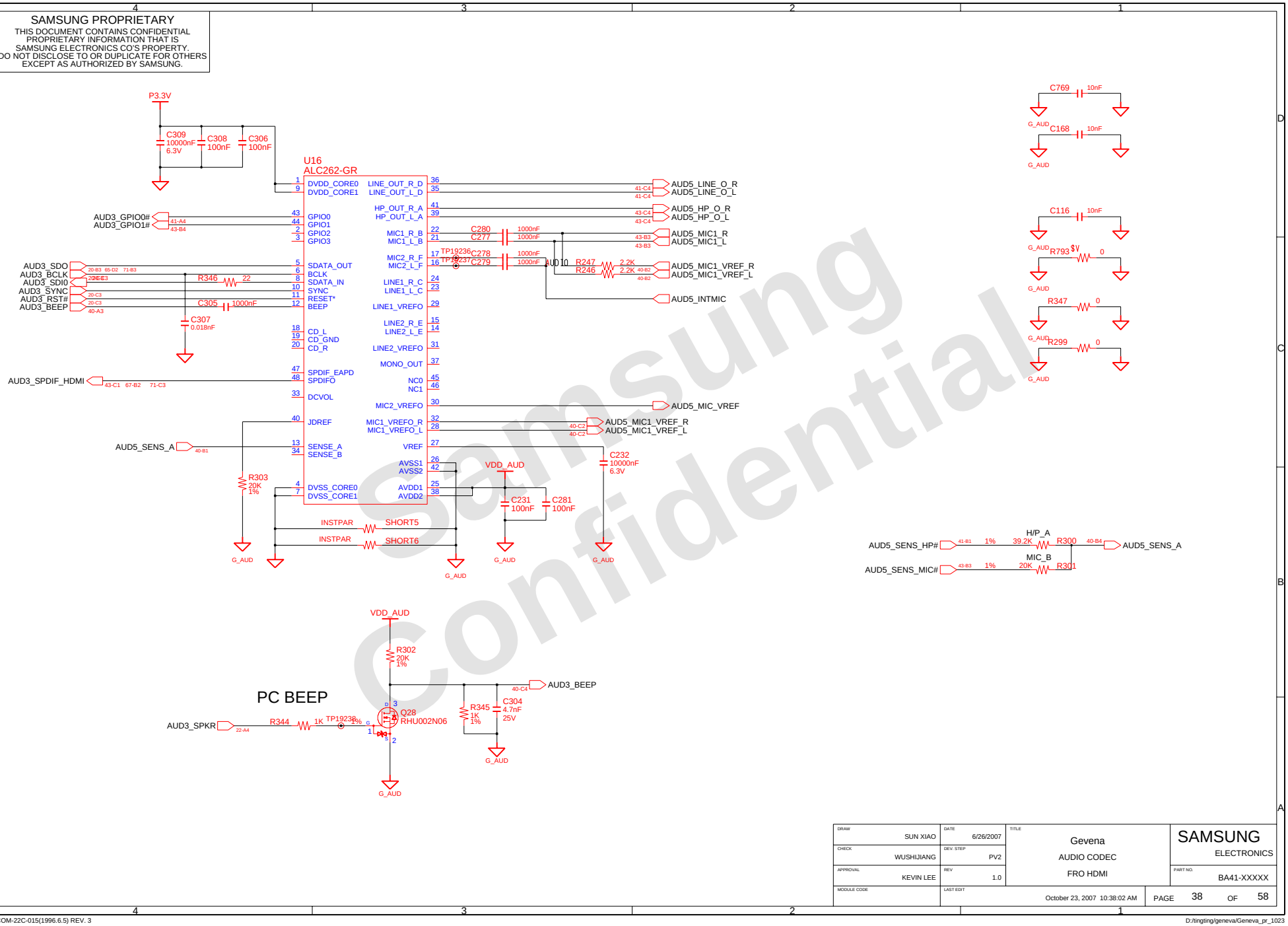
DRAW: SUN XIAO	DATE: 6/26/2007	TITLE: Gevena MINI CARD FRO BOBSON AND DVB-T	SAMSUNG ELECTRONICS
CHECK: WUSHIJIANG	DEV. STEP: PV2		
APPROVAL: KEVIN LEE	REV: 1.0		PART NO.: BA41-XXXXX
MODULE CODE	LAST EDIT: October 23, 2007 10:38:02 AM	PAGE 36 OF 58	



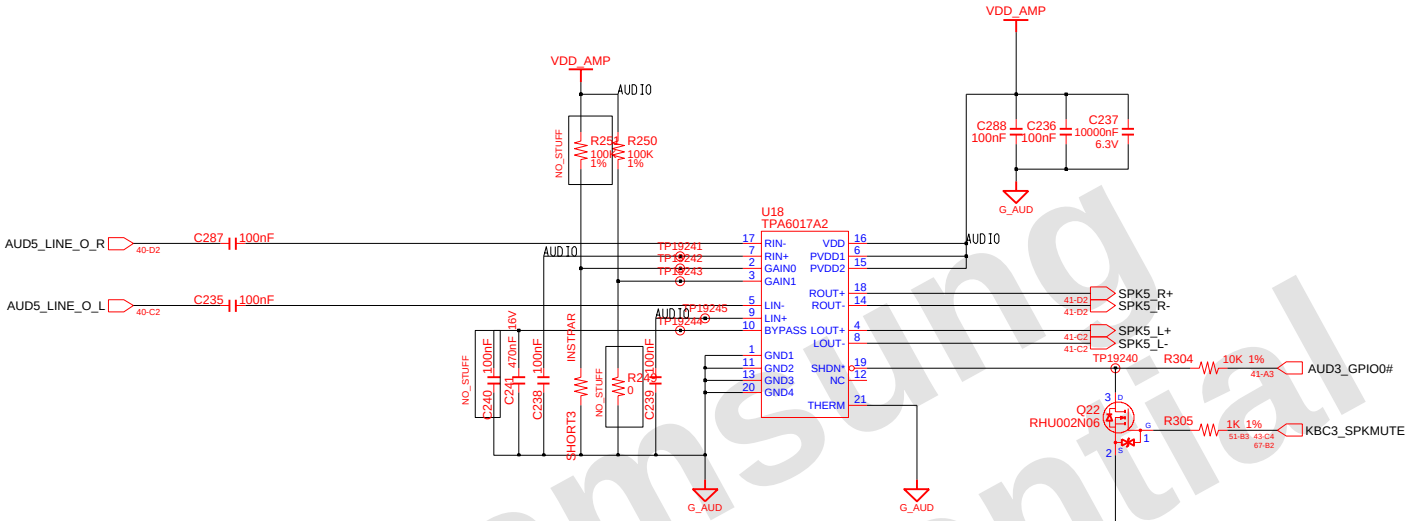




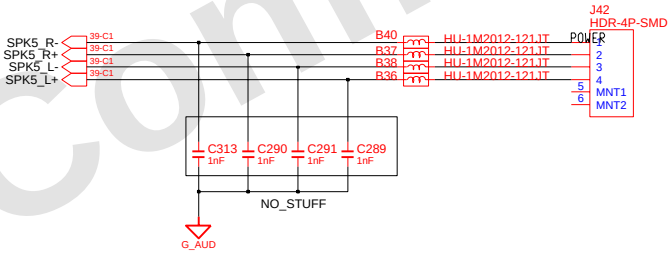
DRAW: SUN XIAO	DATE: 6/27/2007	TITLE: Geneva MIO BOARD EXPRESS CARD	SAMSUNG ELECTRONICS
CHECK: WUSHIJIANG	DEV. STEP: PV2		
APPROVAL: KEVIN LEE	REV: 1.0		PART NO.: BA41-XXXX
MODULE CODE:	LAST EDIT: October 23, 2007 10:38:02 AM	PAGE 37 OF 60	



DRAW: SUN XIAO	DATE: 6/26/2007	TITLE: Gevena AUDIO CODEC FRO HDMI	SAMSUNG ELECTRONICS
CHECK: WUSHIJIANG	DEV. STEP: PV2		
APPROVAL: KEVIN LEE	REV: 1.0		PART NO.: BA41-XXXXX
MODULE CODE	LAST EDIT: October 23, 2007 10:38:02 AM	PAGE 38 OF 58	

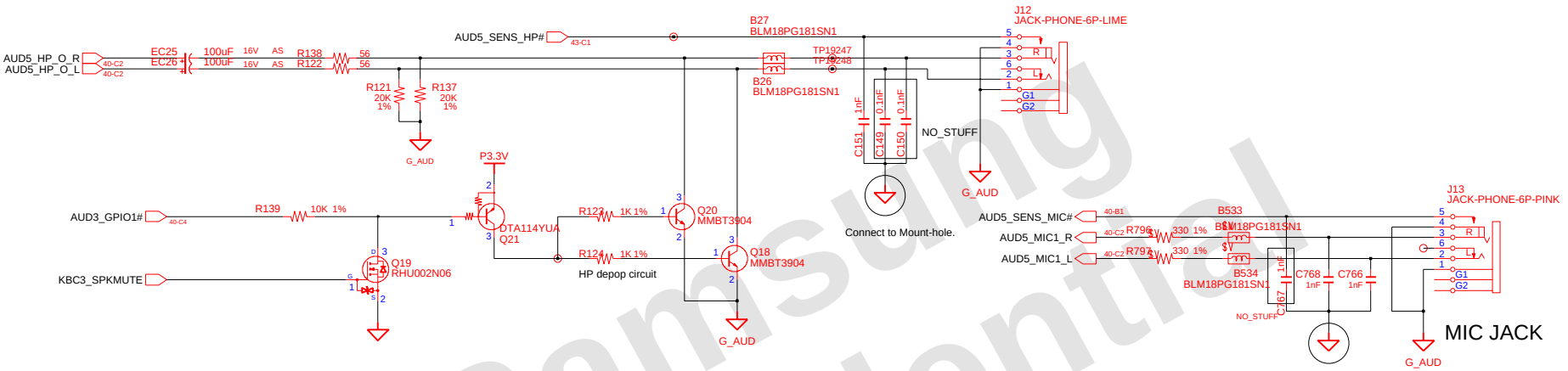


INTERNAL STEREO SPEAKERS



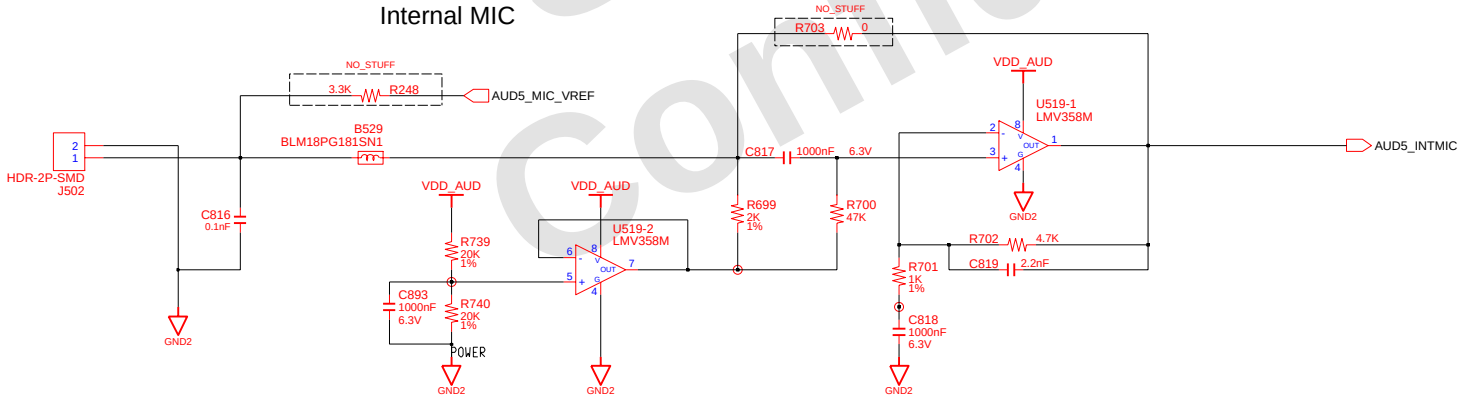
DRAW: SUN XIAO	DATE: 6/26/2007	TITLE: Gevena AUDIO AMP	SAMSUNG ELECTRONICS
CHECK: WUSHIJIANG	DEV. STEP: PV2		
APPROVAL: KEVIN LEE	REV: 1.0		PART NO.: BA41-XXXXX
MODULE CODE	LAST EDIT: October 23, 2007 10:38:02 AM	PAGE 39 OF 58	

HEADPHONE



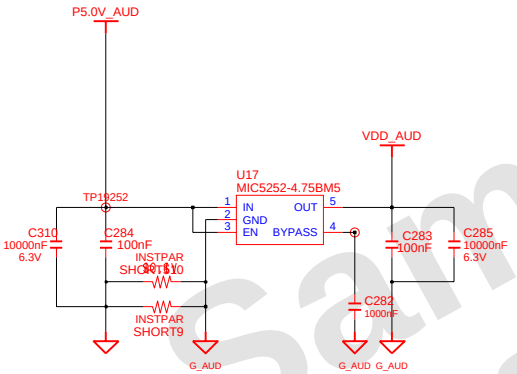
The traces led to Audio Jacks have the width over 10mil

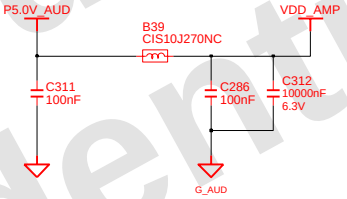
Internal MIC

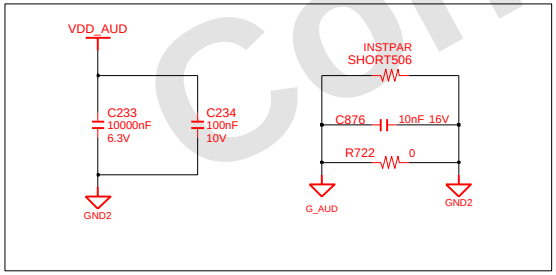


DRAW: SUN XIAO	DATE: 6/26/2007	TITLE: Gevena HEAD PHONE JACK AND MIC JACK	SAMSUNG ELECTRONICS
CHECK: WUSHIJIANG	DEV. STEP: PV2		
APPROVAL: KEVIN LEE	REV: 1.0		PART NO.: BA41-XXXXX
MODULE CODE:	LAST EDIT: October 23, 2007 10:38:02 AM	PAGE 40 OF 58	

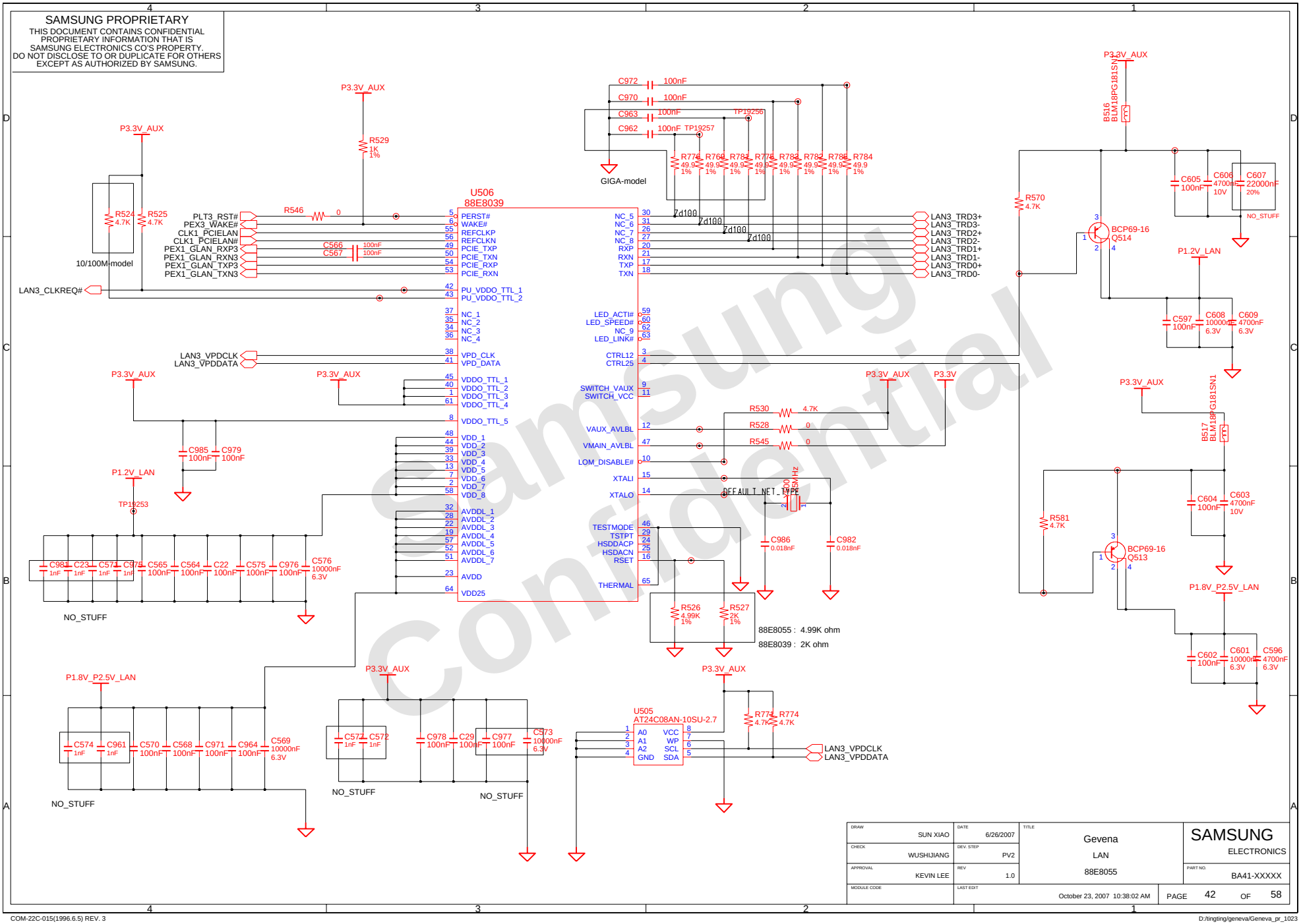
AUDIO POWER



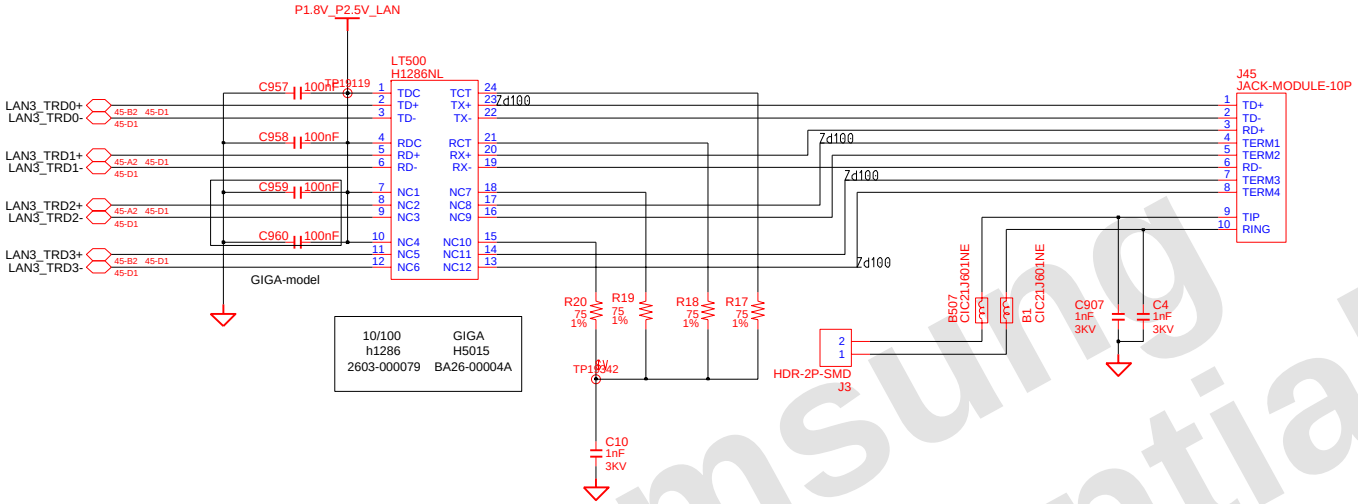




DRAW: SUN XIAO	DATE: 6/26/2007	TITLE: Gevena / AUDIO / AUDIO POWER	SAMSUNG ELECTRONICS
CHECK: WUSHIJIANG	DEV. STEP: PV2		
APPROVAL: KEVIN LEE	REV: 1.0		PART NO.: BA41-XXXXX
MODULE CODE:	LAST EDIT: October 23, 2007 10:38:02 AM	PAGE 41 OF 58	

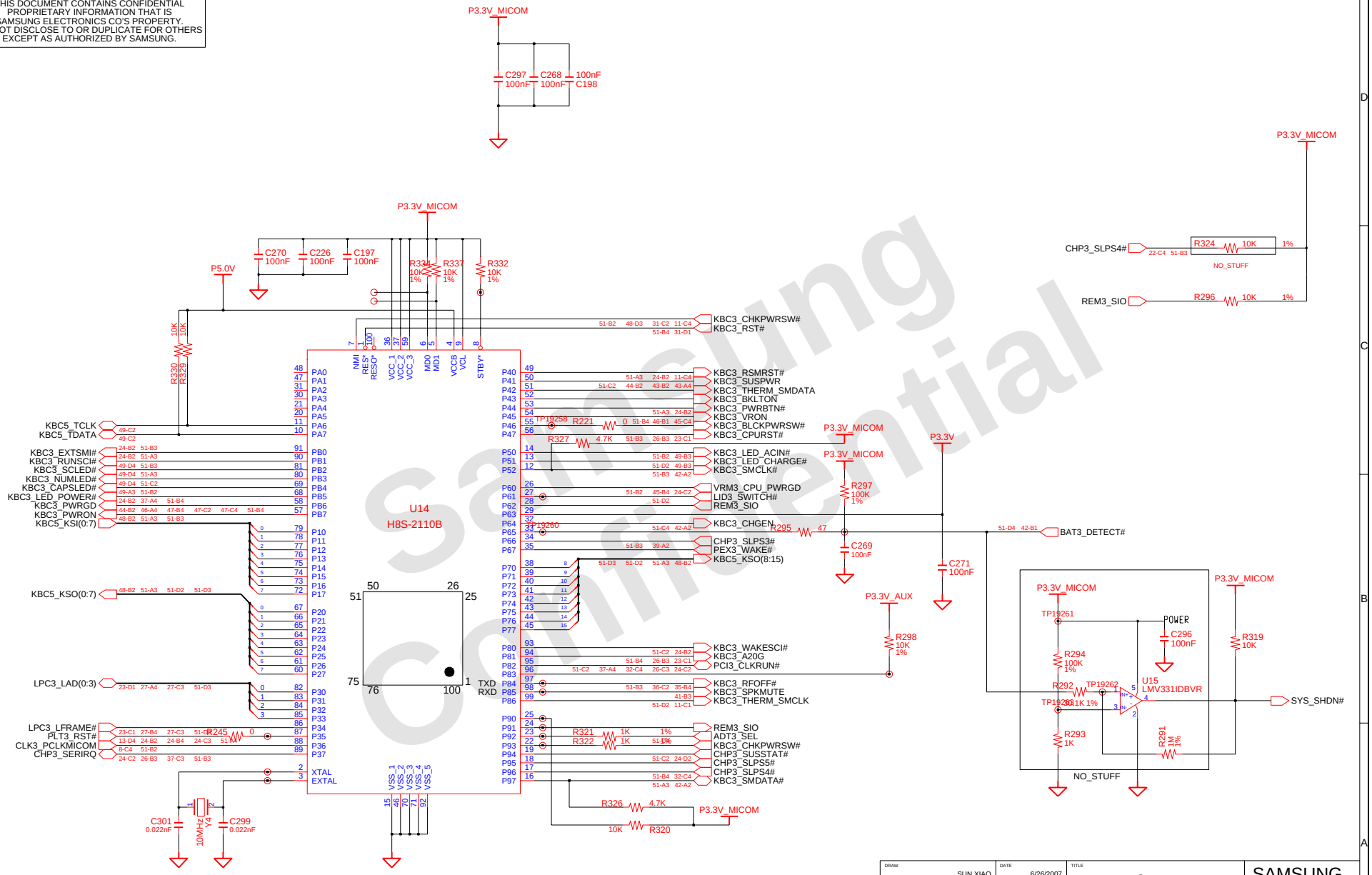


The ditance between LAN controller
and transformer is designed to extend less than two inches.



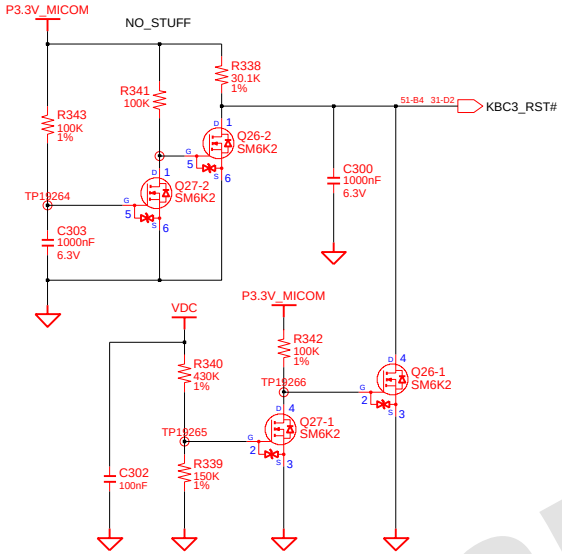
10/100	GIGA
h1286	H5015
2603-000079	BA26-00004A

DRAW: SUN XIAO	DATE: 6/26/2007	TITLE: Gevena / LAN / LAN JACK RJ45	SAMSUNG ELECTRONICS
CHECK: WUSHIJIANG	DEV. STEP: PV2		
APPROVAL: KEVIN LEE	REV: 1.0		PART NO.: BA41-XXXXX
MODULE CODE:	LAST EDIT: October 23, 2007 10:38:02 AM	PAGE 43 OF 58	

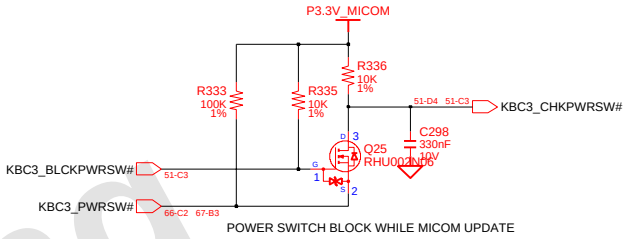


DRAW: SUN XIAO	DATE: 6/26/2007	TITLE: Gevena MICOM 211B	SAMSUNG ELECTRONICS
CHECK: WUSHIJIANG	DEV. STEP: PV2		
APPROVAL: KEVIN LEE	REV: 1.0		PART NO.: BA41-XXXXX
MODULE CODE:	LAST EDIT: October 23, 2007 10:38:02 AM	PAGE 44 OF 58	

MICOM RESET

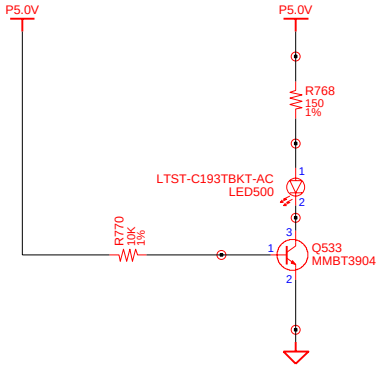


FOR MICOM UPDATE

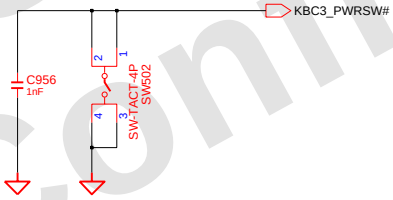


POWER SWITCH BLOCK WHILE MICOM UPDATE

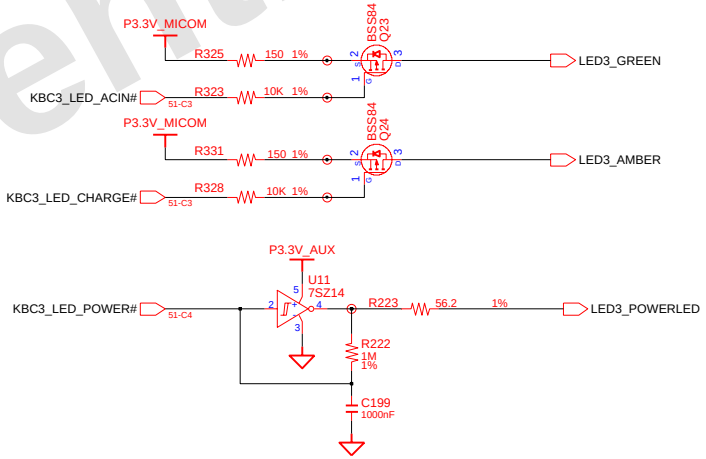
POWER ON LED



POWER ON SW BUTTON

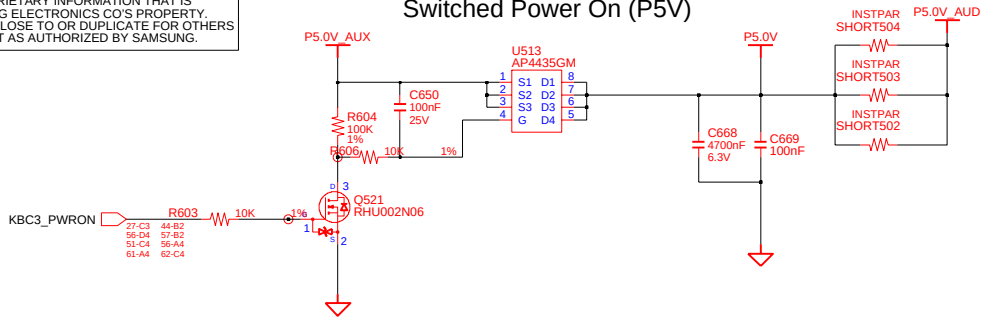


ADAPTERIN/CHARGING LED

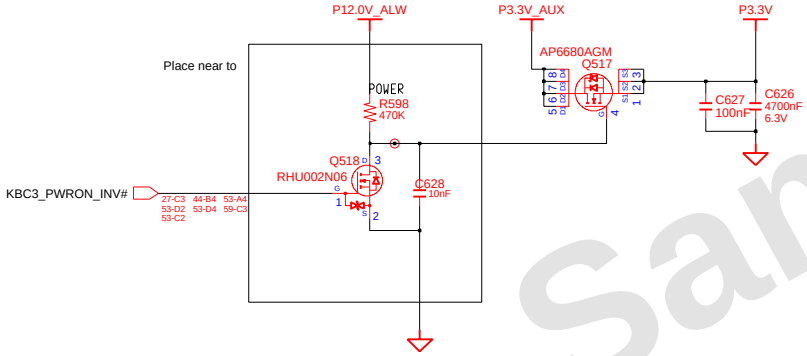


DRAW: SUN XIAO	DATE: 6/26/2007	TITLE: Gevena / MICOM / MICOM LOGIC SCH	SAMSUNG ELECTRONICS
CHECK: WUSHIJIANG	DEV. STEP: PV2		
APPROVAL: KEVIN LEE	REV: 1.0		PART NO.: BA41-XXXXX
MODULE CODE:	LAST EDIT: October 23, 2007 10:38:02 AM	PAGE 45 OF 58	

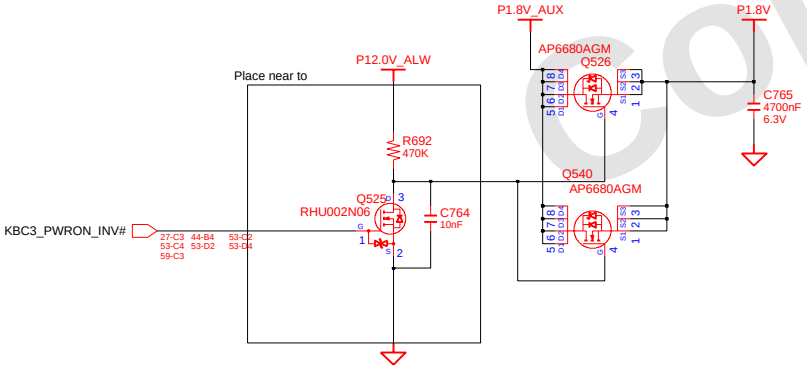
Switched Power On (P5V)



Switched Power On (P3.3V)

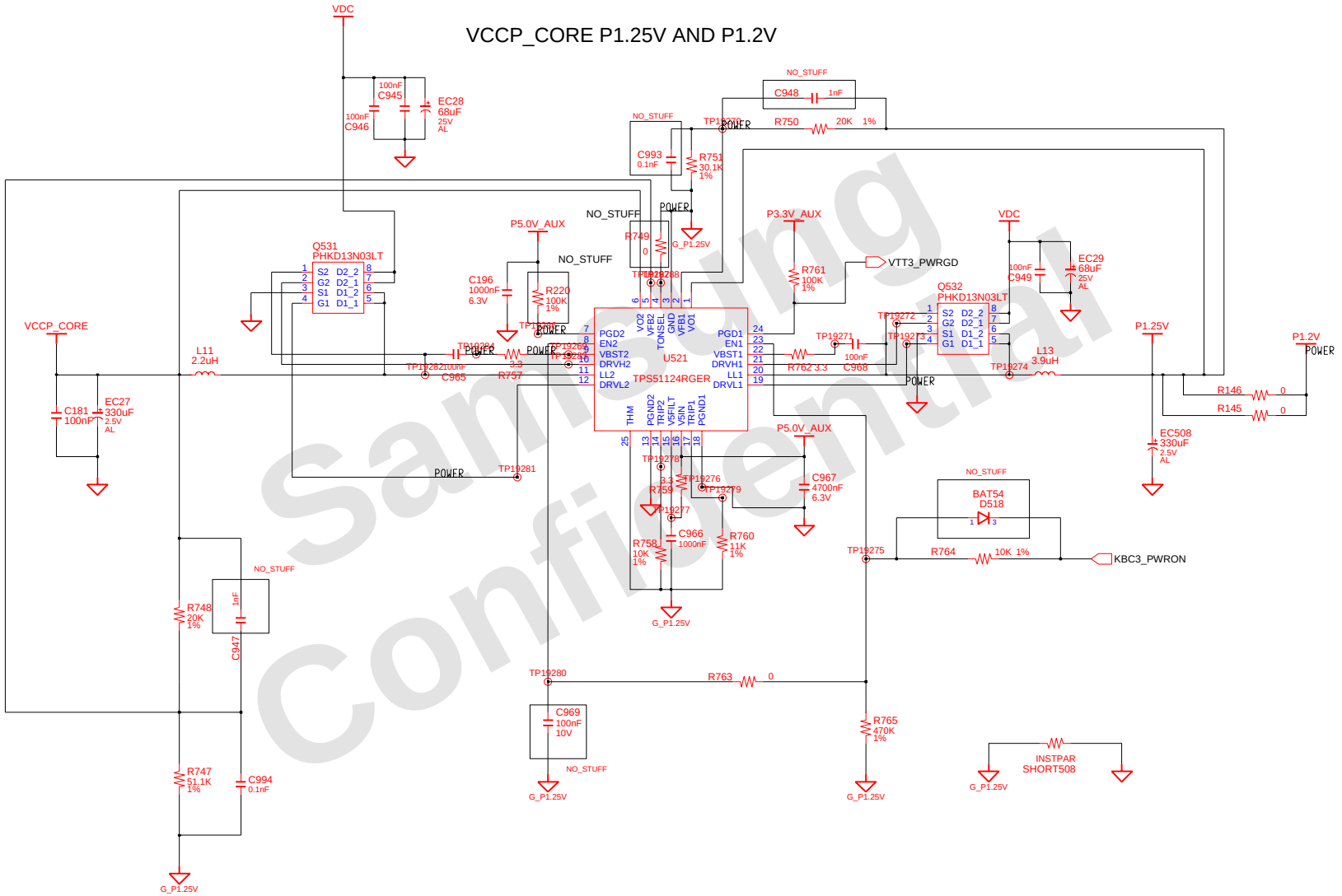


Switched Power On (P1.8V)



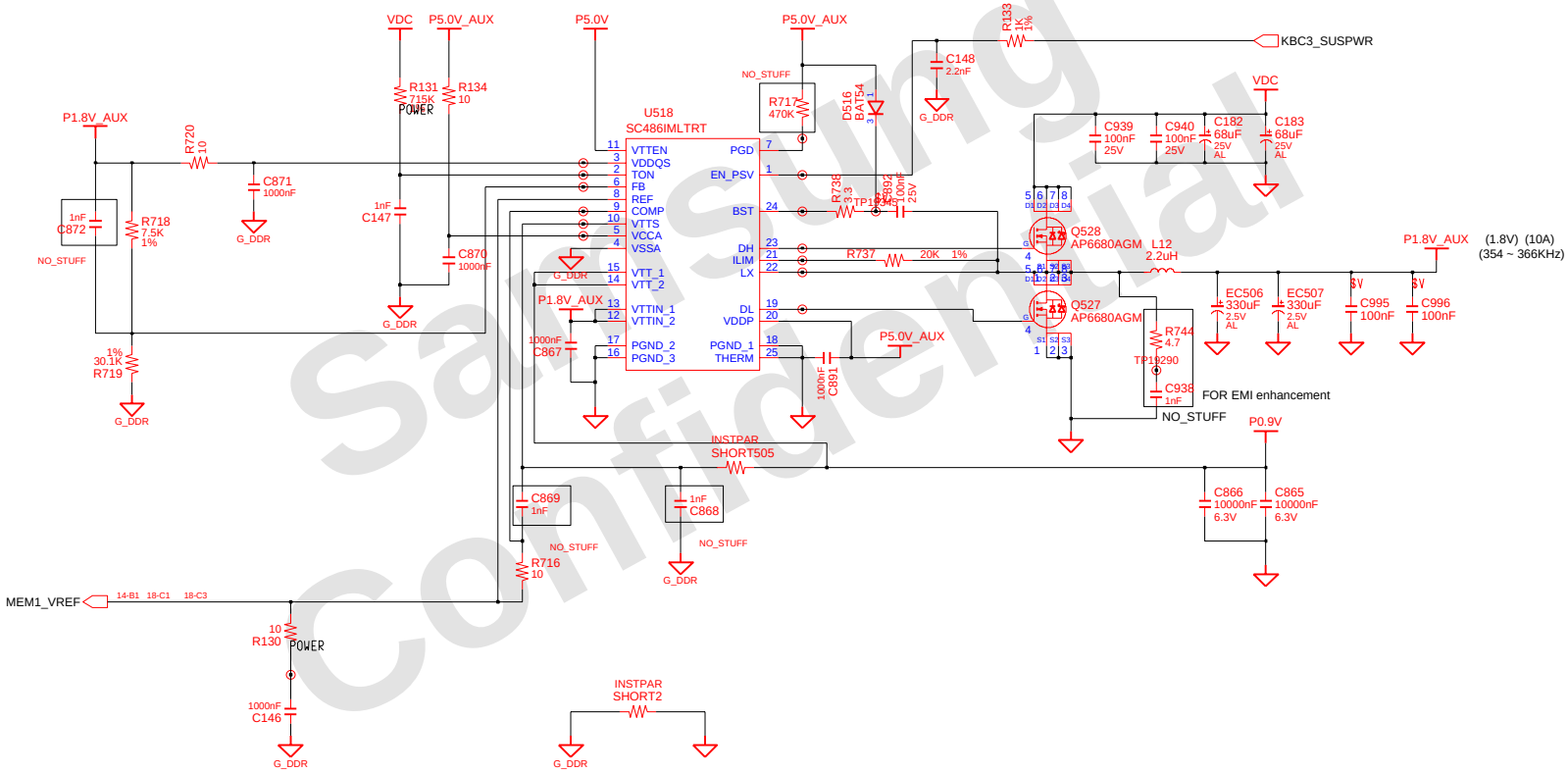
DRAW: SUN XIAO	DATE: 6/26/2007	TITLE: Gevena / MAIN / SWITCH POWER P1.5V	SAMSUNG ELECTRONICS
CHECK: WUSHIJIANG	DEV. STEP: PV2		
APPROVAL: KEVIN LEE	REV: 1.0		PART NO.: BA41-XXXXX
MODULE CODE:	LAST EDIT: October 23, 2007 10:38:02 AM	PAGE 46 OF 58	

VCCP_CORE P1.25V AND P1.2V



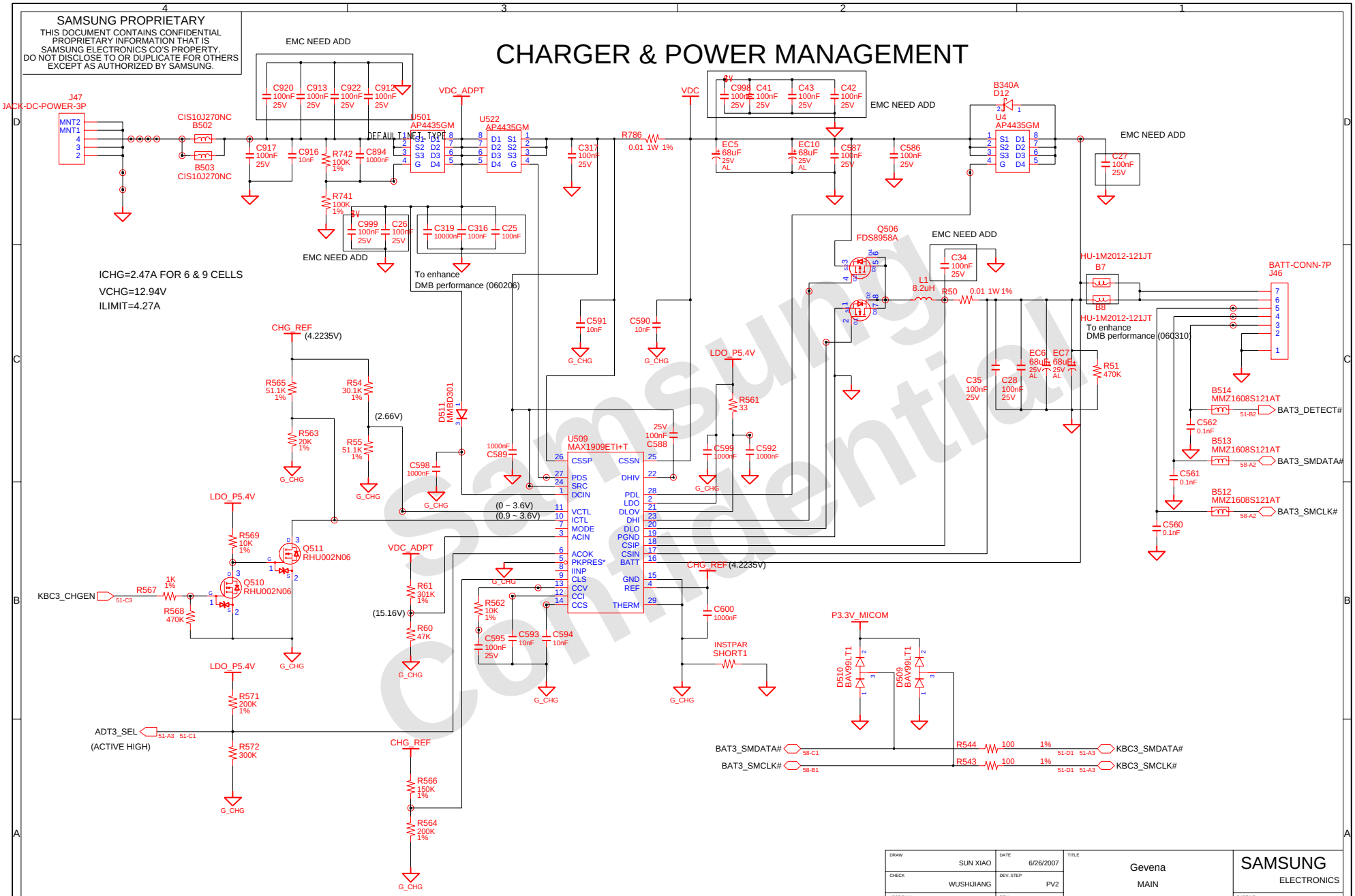
DRAW: SUN XIAO	DATE: 6/26/2007	TITLE: Gevena / MAIN / VCCP P1.25V AND P1.2V	SAMSUNG ELECTRONICS
CHECK: WUSHIJIANG	DEV. STEP: PV2		
APPROVAL: KEVIN LEE	REV: 1.0		PART NO.: BA41-XXXXX
MODULE CODE:	LAST EDIT: October 23, 2007 10:38:02 AM	PAGE 47 OF 58	

DDR2 Power



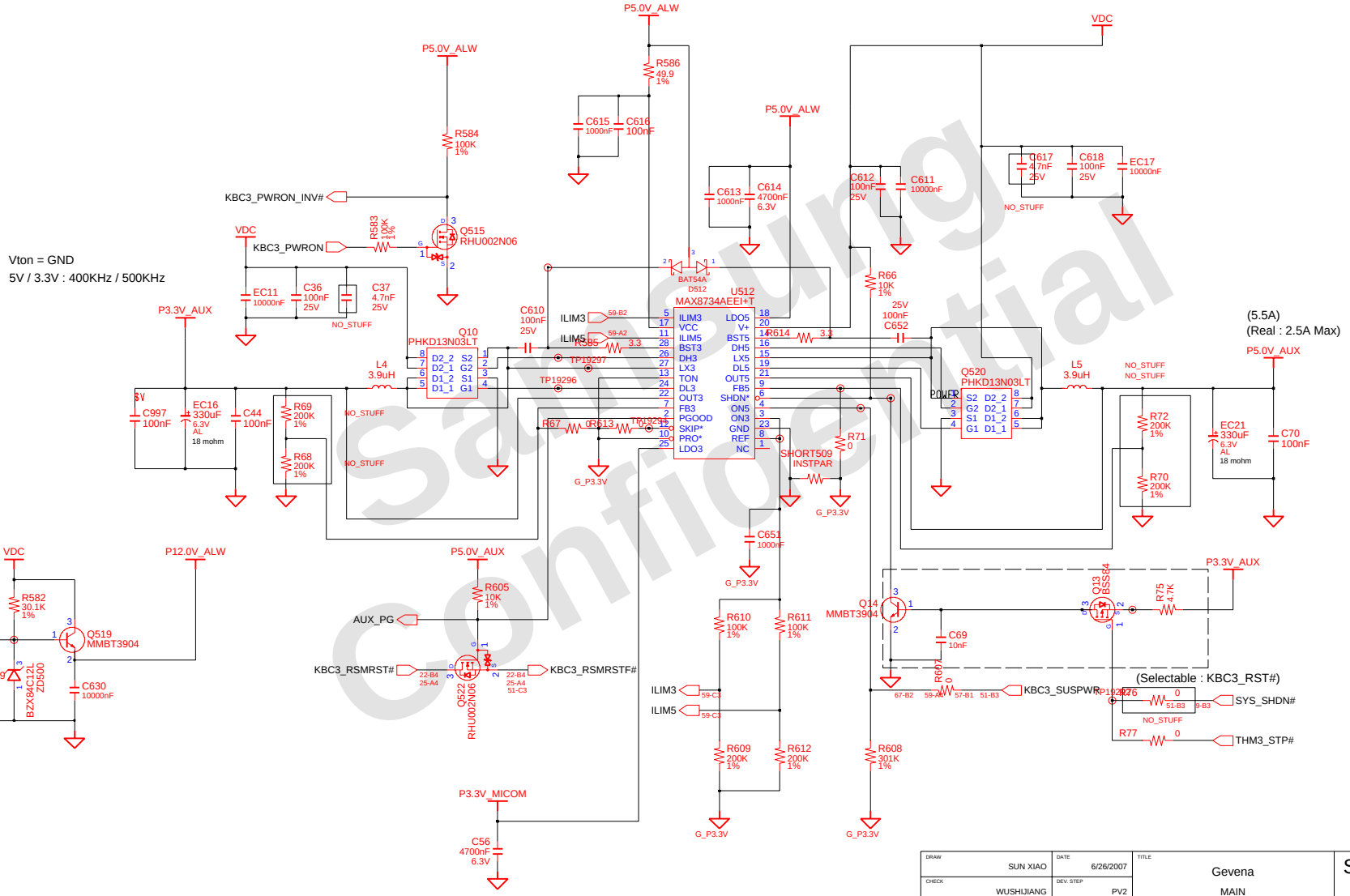
DRAW: SUN XIAO	DATE: 6/26/2007	TITLE: Gevena / MAIN / DDR2 POWER	SAMSUNG ELECTRONICS
CHECK: WUSHIJIANG	DEV. STEP: PV2		
APPROVAL: KEVIN LEE	REV: 1.0		PART NO.: BA41-XXXXX
MODULE CODE:	LAST EDIT: October 23, 2007 10:38:02 AM	PAGE 48 OF 58	

CHARGER & POWER MANAGEMENT



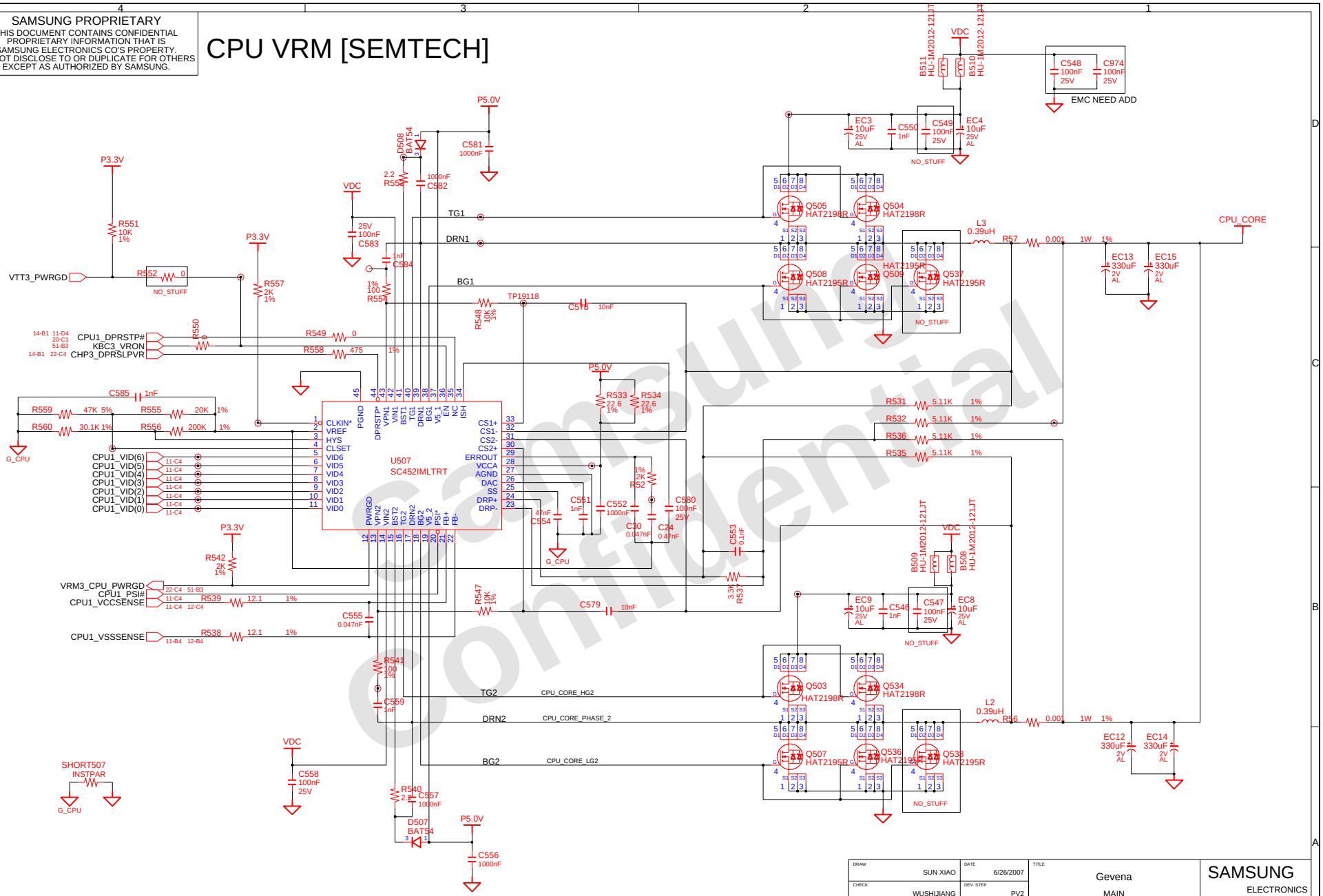
DRAW: SUN XIAO	DATE: 6/26/2007	TITLE: Gevena / MAIN / CHARGE & BATTERY CONN	SAMSUNG ELECTRONICS
CHECK: WUSHIJIANG	DEV. STEP: PV2		
APPROVAL: KEVIN LEE	REV: 1.0		PART NO.: BA41-XXXXX
MODULE CODE:	LAST EDIT: October 23, 2007 10:38:02 AM	PAGE 49 OF 58	

P3.3V_ALW/AUX & P5V_AUX



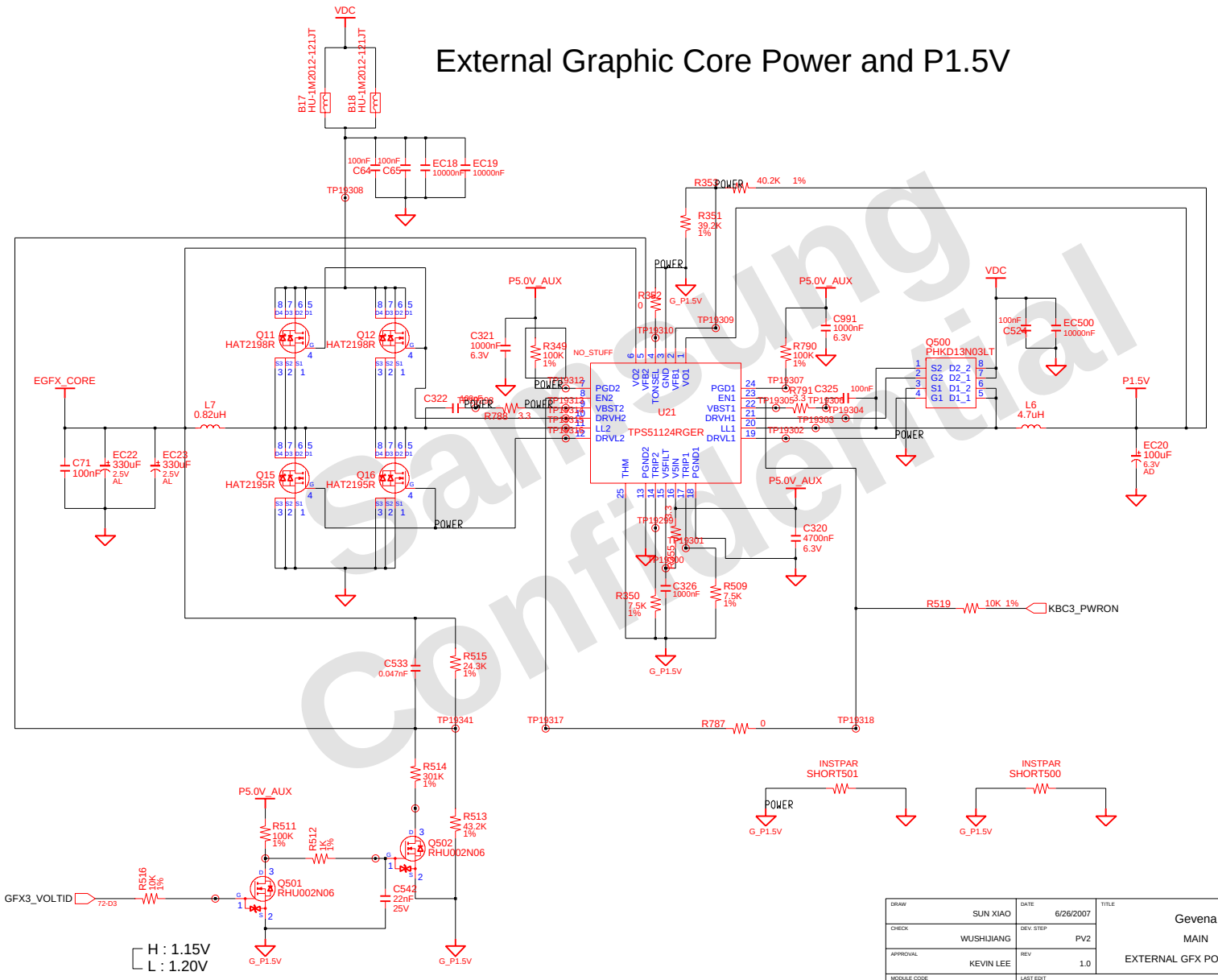
DRAW: SUN XIAO	DATE: 6/26/2007	TITLE: Gevena	SAMSUNG ELECTRONICS
CHECK: WUSHIJIANG	DEV. STEP: PV2	MAIN	
APPROVAL: KEVIN LEE	REV: 1.0	P3.3V_ALW/AUX & P5.0V_ALW	PART NO.: BA41-XXXXX
MODULE CODE	LAST EDIT: October 23, 2007 10:38:02 AM	PAGE 50 OF 58	

CPU VRM [SEMTECH]

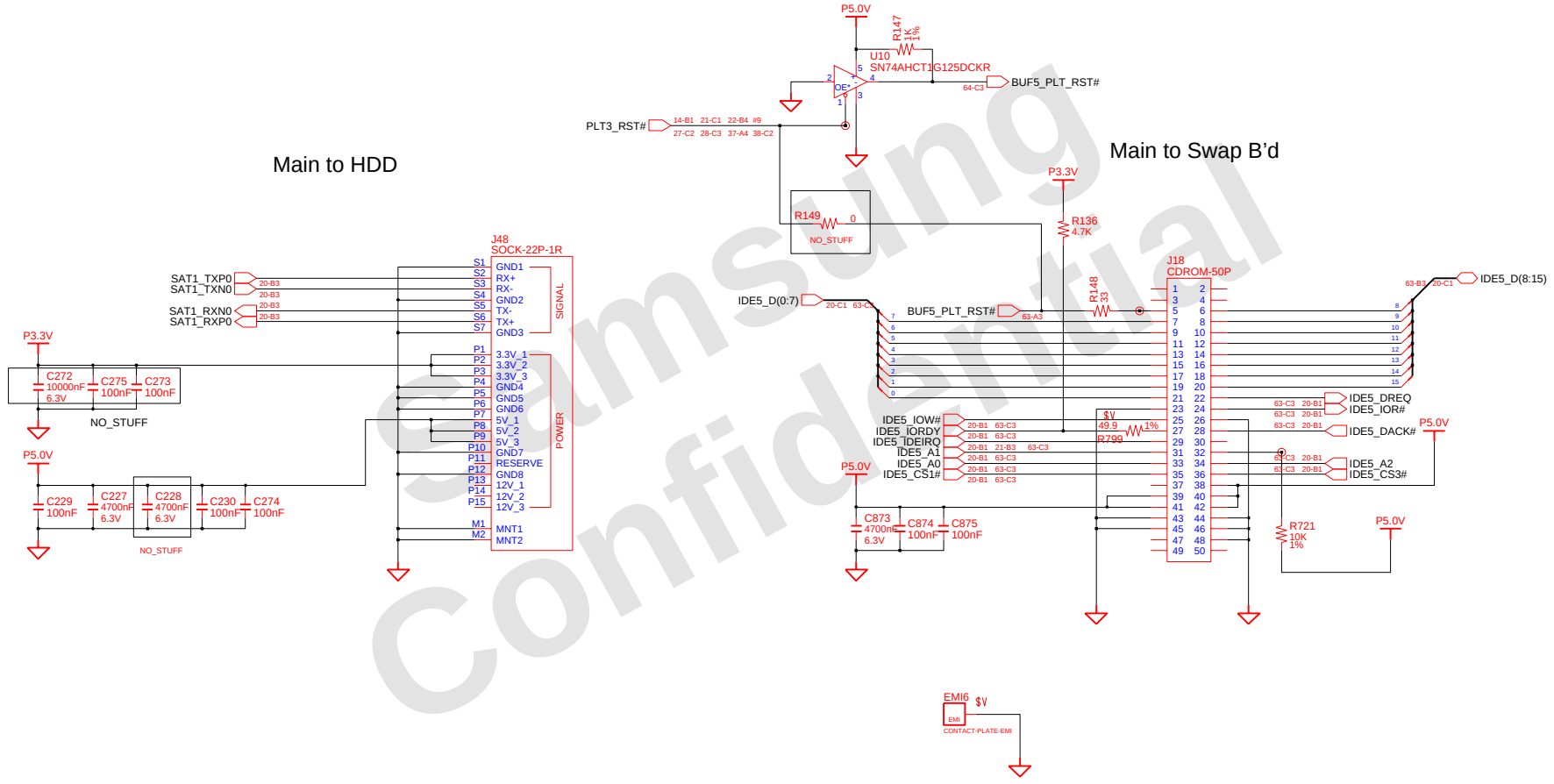


DRAW: SUN XIAO	DATE: 6/26/2007	TITLE: Gevena MAIN CPU VRM	SAMSUNG ELECTRONICS
CHECK: WUSHIJIANG	DEV. STEP: PV2		
APPROVAL: KEVIN LEE	REV: 1.0		PART NO.: BA41-XXXXX
MODULE CODE:	LAST EDIT: October 23, 2007 10:38:02 AM	PAGE 51 OF 58	

External Graphic Core Power and P1.5V



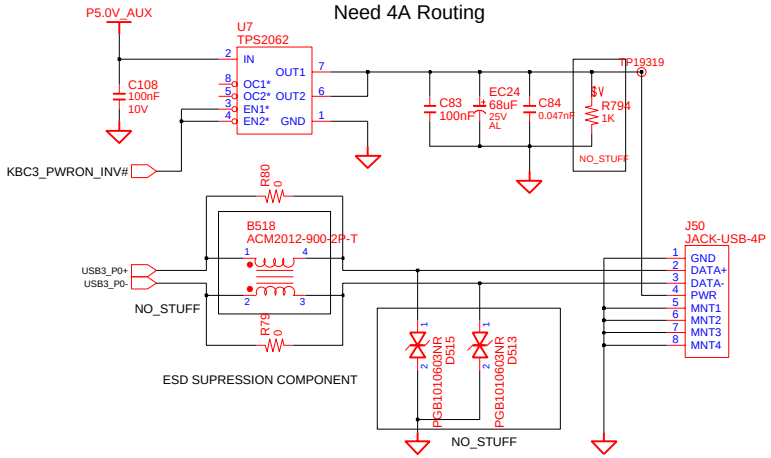
DRAW: SUN XIAO	DATE: 6/26/2007	TITLE: Gevena / MAIN / EXTERNAL GFX POWER VRM	SAMSUNG ELECTRONICS
CHECK: WUSHIJIANG	DEV. STEP: PV2		
APPROVAL: KEVIN LEE	REV: 1.0		PART NO.: BA41-XXXXX
MODULE CODE:	LAST EDIT: October 23, 2007 10:38:02 AM	PAGE 52 OF 58	



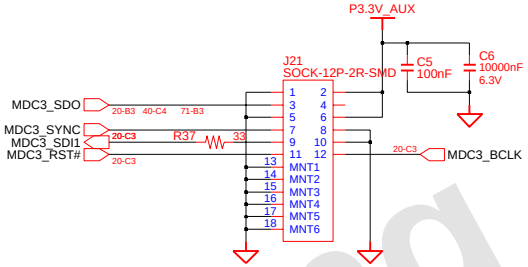
DRAW: SUN XIAO	DATE: 6/26/2007	TITLE: Gevena CONNECTOR HDD & ODD CONNECTOR	SAMSUNG ELECTRONICS
CHECK: WUSHIJIANG	DEV. STEP: PV2		
APPROVAL: KEVIN LEE	REV: 1.0		PART NO.: BA41-XXXXX
MODULE CODE:	LAST EDIT: October 23, 2007 10:38:02 AM	PAGE 53 OF 58	

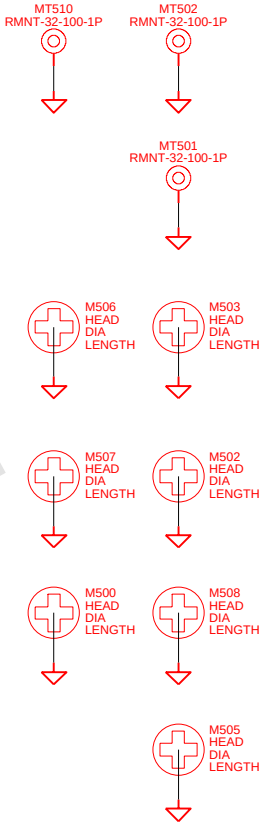
1 PORT USB CONNECTOR

Need 4A Routing

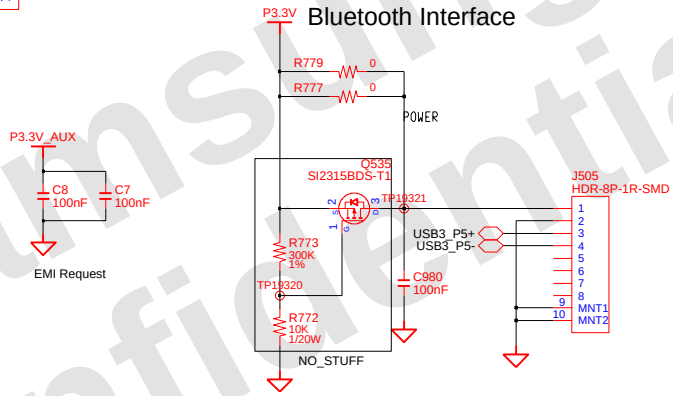


MDC Connecter



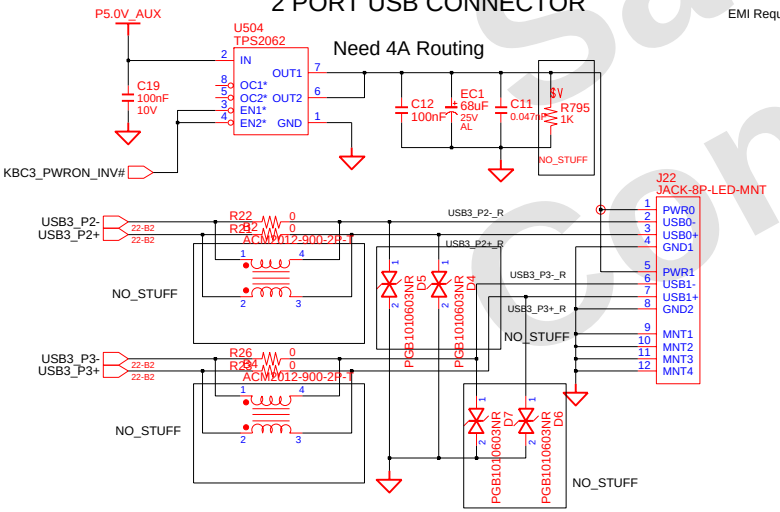


Bluetooth Interface

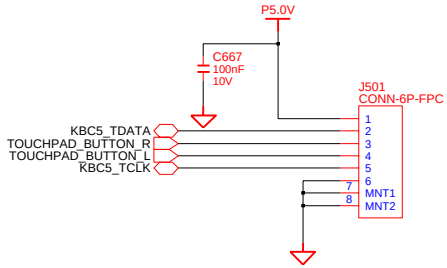


2 PORT USB CONNECTOR

Need 4A Routing

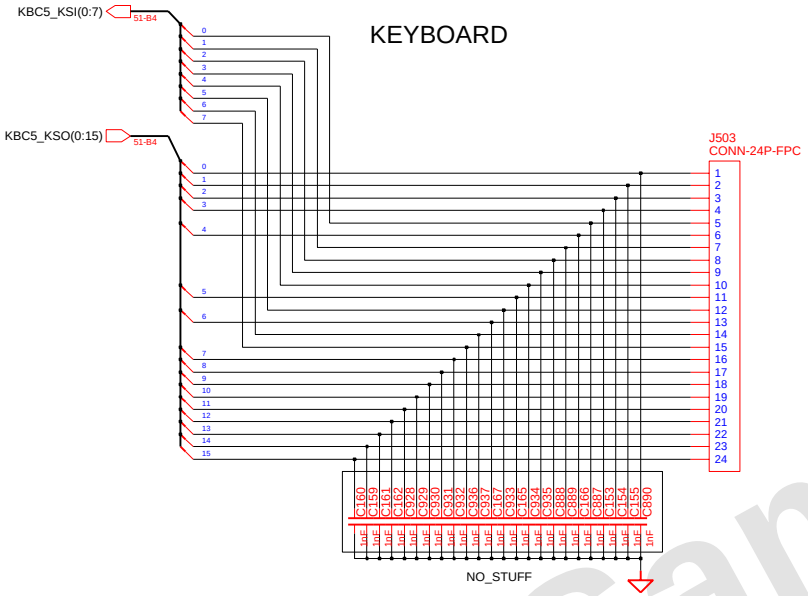


TOUCHPAD CONNECTOR

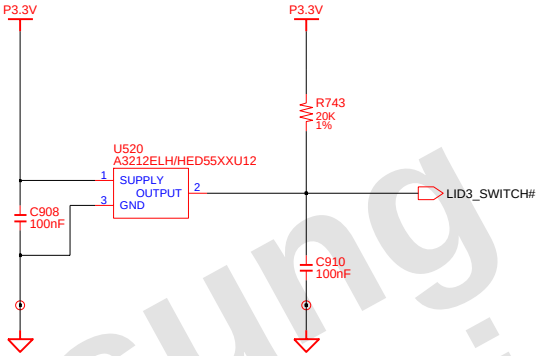


DRAW: SUN XIAO	DATE: 6/26/2007	TITLE: Gevena USB MDC & TOUCHPAD BLUETOOTH I/F	SAMSUNG ELECTRONICS
CHECK: WUSHIJIANG	DEV. STEP: PV2		
APPROVAL: KEVIN LEE	REV: 1.0		PART NO.: BA41-XXXXX
MODULE CODE	LAST EDIT: October 23, 2007 10:38:02 AM	PAGE 54 OF 58	

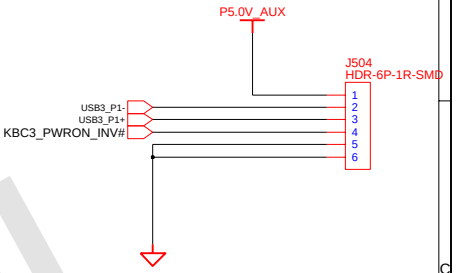
KEYBOARD



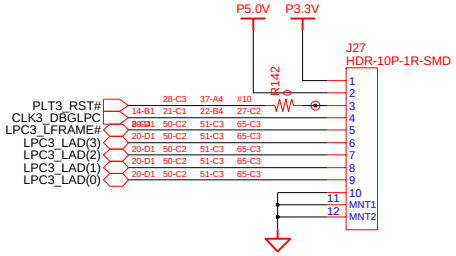
LID_SWITCH



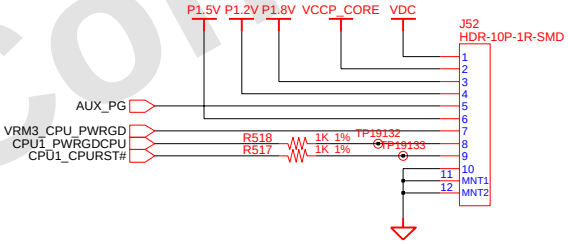
USB I/F B'D



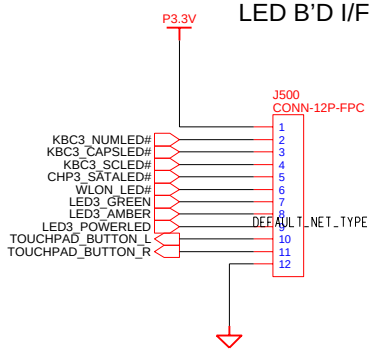
80H DECODER CONNECTOR



ICT PORT

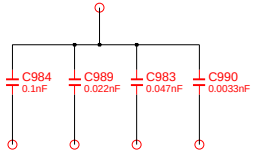


LED B'D I/F

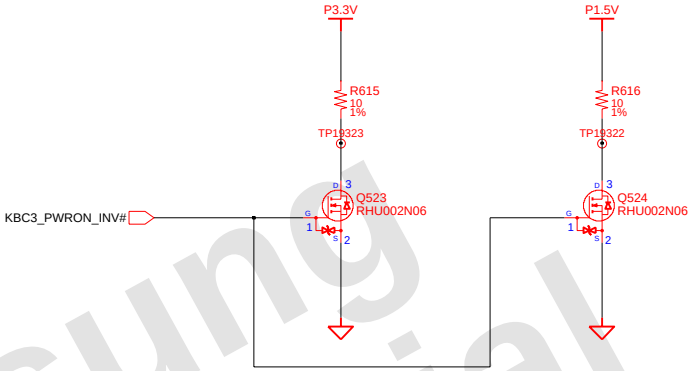


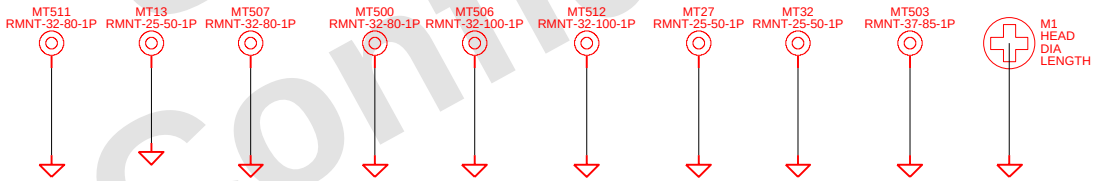
DRAW: SUN XIAO	DATE: 6/26/2007	TITLE: Gevena KEYBOARD 80PORT ICT PORT LID SWITCH LED B'D USB I/O B'D	SAMSUNG ELECTRONICS
CHECK: WUSHIJIANG	DEV. STEP: PV2		
APPROVAL: KEVIN LEE	REV: 1.0		PART NO.: BA41-XXXXX
MODULE CODE:	LAST EDIT: October 23, 2007 10:38:02 AM	PAGE 55 OF 58	

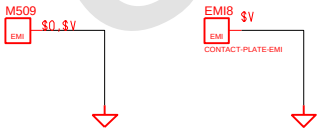
TOP SIDE



BOTTOM SIDE

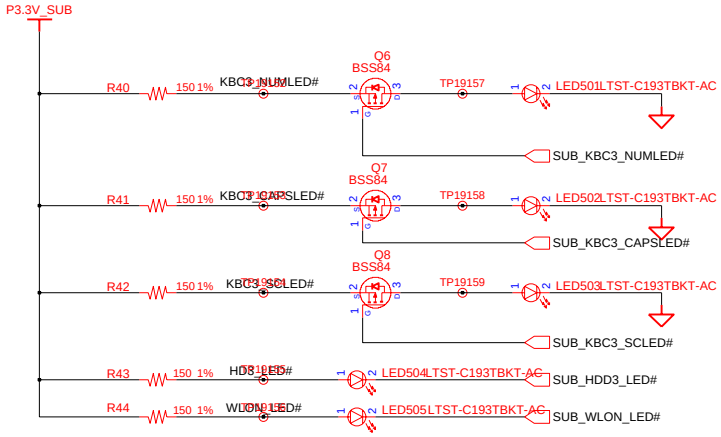


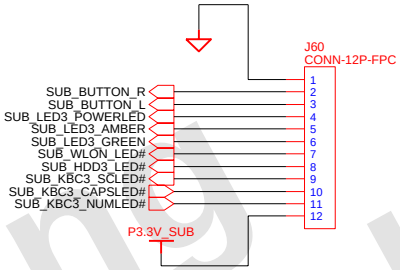


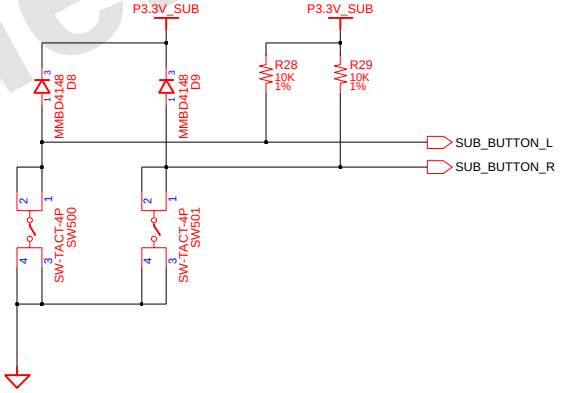


DRAW: SUN XIAO	DATE: 6/26/2007	TITLE: Gevena OTHERS	SAMSUNG ELECTRONICS
CHECK: WUSHIJIANG	DEV. STEP: PV2		
APPROVAL: KEVIN LEE	REV: 1.0		PART NO.: BA41-XXXXX
MODULE CODE:	LAST EDIT: October 23, 2007 10:38:02 AM	PAGE 56 OF 58	

TOUCHPAD AND LED B'D

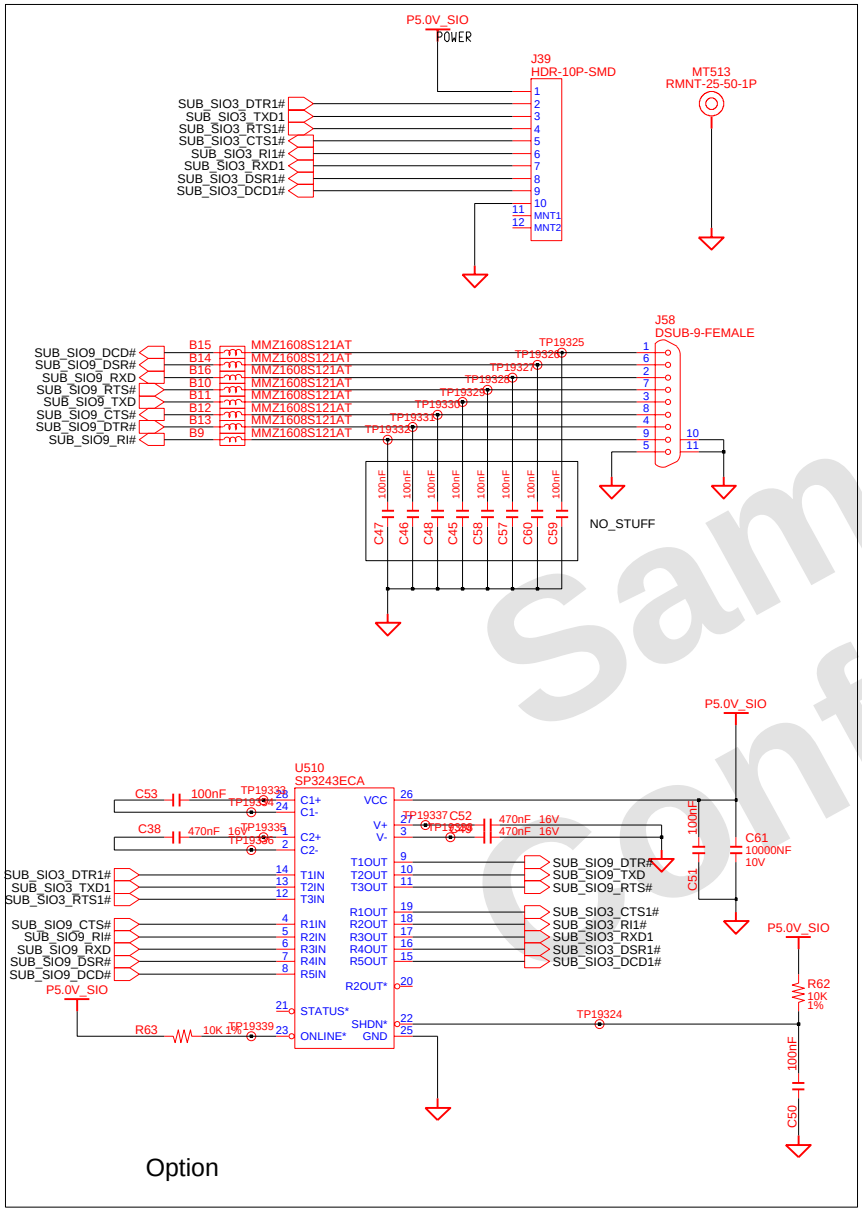


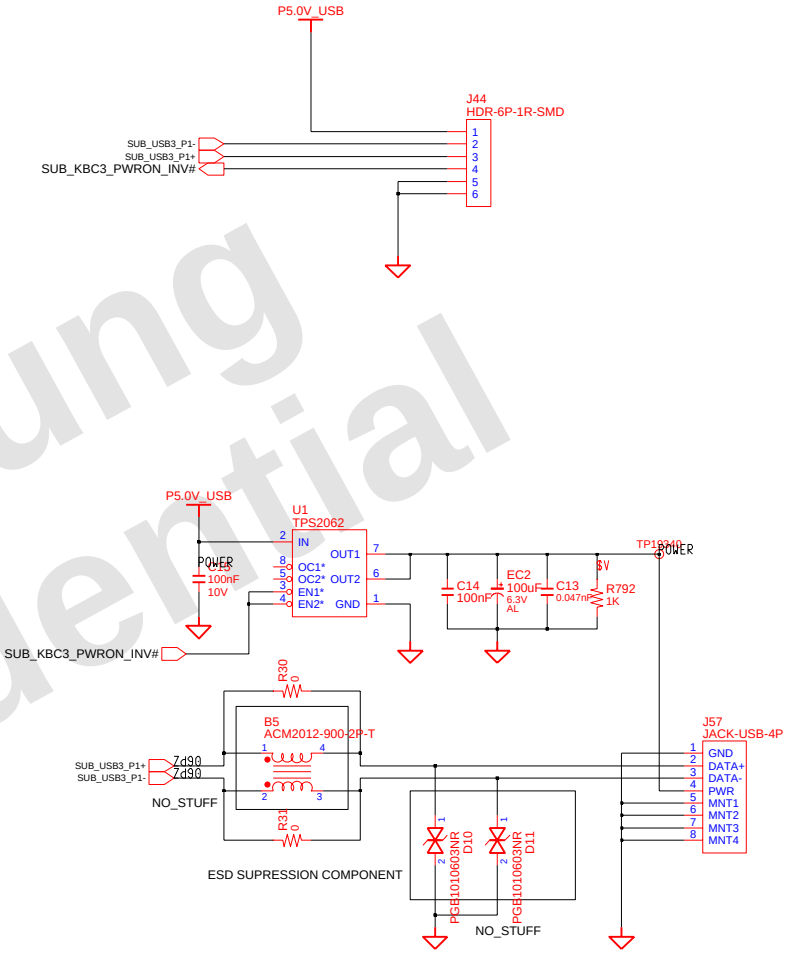




DRAW: SUN XIAO	DATE: 6/26/2007	TITLE: Gevena TOUCHPAD AND LED B'D	SAMSUNG ELECTRONICS
CHECK: WUSHIJIANG	DEV. STEP: PV2		
APPROVAL: KEVIN LEE	REV: 1.0		PART NO.: BA41-
MODULE CODE:	LAST EDIT: October 23, 2007 10:38:02 AM	PAGE 57 OF 60	

SIO AND USB SUB B'D





DRAW: SUN XIAO	DATE: 6/30/2007	TITLE: Geneva MIO BOARD USB AND SIO SUB B'D	SAMSUNG ELECTRONICS
CHECK: WUSHIJIANG	DEV. STEP: PV2		
APPROVAL: KEVIN LEE	REV: 1.0		PART NO.: BA41-undefined
MODULE CODE:	LAST EDIT: October 23, 2007 10:38:02 AM	PAGE 58 OF 60	

TP18380 ADT3_SEL
TP18381 AUD3_BCLK
TP18382 AUD3_BEEP
TP18383 AUD3_BEEP_CU
TP18384 AUD3_GPIO0#
TP18385 AUD3_GPIO1#
TP18386 AUD3_GPIO1#_U
TP18387 AUD3_RST#
TP18388 AUD3_SDI0
TP18389 AUD3_SDI0_RU
TP18390 AUD3_SDO
TP18391 AUD3_SPKR

TP18393 AUD3_SYNC
TP18394 AUD5_HP_O_L
TP18395 AUD5_HP_O_L_CR
TP18396 AUD5_HP_O_L_RB
TP18397 AUD5_HP_O_R
TP18398 AUD5_HP_O_R_CR
TP18399 AUD5_HP_O_R_RB
TP18400 AUD5_INTMIC
TP18401 AUD5_LINE_O_L
TP18402 AUD5_LINE_O_L_CU
TP18403 AUD5_LINE_O_R
TP18404 AUD5_LINE_O_R_CU
TP18405 AUD5_MIC1_L
TP18406 AUD5_MIC1_L_BCON
TP18407 AUD5_MIC1_L_CU
TP18408 AUD5_MIC1_R
TP18409 AUD5_MIC1_R_BCON
TP18410 AUD5_MIC1_R_CU
TP18411 AUD5_MIC1_VREF_L
TP18348 AUD5_MIC1_VREF_R
TP18349 AUD5_MIC_VREF
TP18350 AUD5_SENS_A
TP18351 AUD5_SENS_MIC#
TP18352 AUD_JDREF_R
TP18353 AUD_VREF
TP18354 AUX_PG

TP18361 BAT3_SMCLK#
TP18362 BAT3_SMDATA#
TP18363 BATT_CONN_7P_BB
TP18364 BUF5_PLT_RST#

TP18367 CHP1.5_DMICOMP_R
TP18368 CHP3_BIOSWP#
TP18369 CHP3_BIOS_CRI#
TP18370 CHP3_CL_CLK_0
TP18371 CHP3_CL_DATA_0
TP18372 CHP3_CL_RST#_0
TP18373 CHP3_CL_RST#_1
TP18374 CHP3_CPUSTP#
TP18375 CHP3_CPUSTP#_R_ICH
TP18376 CHP3_DPRSLPVR
TP18377 CHP3_DPRSLPVR_R_ICH
TP18378 CHP3_EXTGFX#
TP18379 CHP3_GPIO12
TP18328 CHP3_GPIO17
TP18329 CHP3_INTRUDER#
TP18330 CHP3_INTVRMEN
TP18331 CHP3_LAN100_SLP
TP18332 CHP3_LDRQ0#
TP18333 CHP3_LDRQ1#
TP18334 CHP3_PCISTP#
TP18335 CHP3_RI#_R
TP18336 CHP3_RTCRST#
TP18337 CHP3_SATACLKREQ#
TP18338 CHP3_SATALED#
TP18339 CHP3_SERIRQ
TP18340 CHP3_SLPS3#
TP18341 CHP3_SLPS4#
TP18342 CHP3_SLPS5#
TP18343 CHP3_SUSSTAT#

TP18344 CHP3_TP7_R
TP18345 CHP3_USBRBIAS_R
TP18346 CHP3_USBROC9#_R
TP18347 CHP_SDATAOUT0_R
TP18319 CLK3_DBGLPC
TP18320 CLK3_ICH14
TP18321 CLK3_PCLKICH
TP18322 CLK3_PCLKMICOM
TP18323 CLK3_PCLKSIO
TP18324 CLK3_PCLKSIO_DS
TP18325 CLK3_PWRGD
TP18326 CLK3_SIO14
TP18327 CLK3_USB48
TP18315 CPU1_A20M#
TP18316 CPU1_ADS#
TP18317 CPU1_BNR#
TP18318 CPU1_BPRI#
TP18306 CPU1_BREQ#
TP18307 CPU1_BSEL0
TP18308 CPU1_BSEL1
TP18309 CPU1_BSEL2
TP18310 CPU1_COMP0_R
TP18311 CPU1_COMP1_R
TP18312 CPU1_COMP2_R
TP18313 CPU1_COMP3_R
TP18314 CPU1_CPURST#

TP18295 CPU1_DBSY#
TP18296 CPU1_DEFER#
TP18297 CPU1_DPRSTP#
TP18298 CPU1_DPSLP#
TP18299 CPU1_DPWR#
TP18300 CPU1_DRDY#
TP18301 CPU1_FERR#
TP18302 CPU1_HIT#
TP18303 CPU1_HITM#
TP18304 CPU1_IERR#
TP18305 CPU1_IGNNE#
TP18259 CPU1_INIT#
TP18260 CPU1_INTR
TP18261 CPU1_LOCK#
TP18262 CPU1_NMI
TP18263 CPU1_PSI#
TP18264 CPU1_PWRGDCPU
TP18270 CPU1_RS0#
TP18271 CPU1_RS1#
TP18272 CPU1_RS2#
TP18273 CPU1_SLP#
TP18274 CPU1_SMI#
TP18275 CPU1_STPCLK#
TP18276 CPU1_TCK
TP18277 CPU1_TDI
TP18278 CPU1_TEST1_R
TP18279 CPU1_TEST2_R
TP18280 CPU1_TEST3_R
TP18281 CPU1_TEST4_R
TP18282 CPU1_TEST5_R
TP18283 CPU1_THRMTRIP#
TP18284 CPU1_THRMTRIP#_R
TP18285 CPU1_TMS
TP18286 CPU1_TRDY#
TP18287 CPU1_TRST#
TP18288 CPU1_VCCSENSE
TP18289 CPU1_VSSSENSE
TP18290 CPU2_THERMDA
TP18251 CPU2_THERMDC
TP18252 CPU3_THRMTRIP#
TP18253 CPU_CORE_HG2
TP18254 CPU_CORE_LG1
TP18255 CPU_CORE_LG2
TP18256 CPU_CORE_PHASE_2

TP17811 DRAM_RSTA#
TP17812 DRAM_RSTC#
TP17813 EDID_CLK
TP17814 EDID_DATA
TP17815 EXP3_CLKREQ#
TP17816 EXP3_CPPE#
TP17817 EXP3_CPUSB#
TP17818 EXP3_PERST#
TP17819 FAN3_FDBACK#
TP17820 FAN5_VDD
TP17821 GFX3_BLON
TP17822 GFX3_BRIT

TP17799 GFX3_HSYNC
TP17800 GFX3_LCDVDDON
TP17801 GFX3_THERM#
TP17802 GFX3_THRMDN
TP17803 GFX3_THRMDP
TP17804 GFX3_VQLTID
TP17805 GFX3_VSYNC

TP17808 IDE5_CS1#
TP17809 IDE5_CS3#
TP17810 IDE5_DACK#
TP17767 IDE5_DREQ
TP17768 IDE5_IDEIRQ
TP17769 IDE5_IOR#
TP17770 IDE5_IORDY
TP17771 IDE5_IOW#
TP17772 ILIM3
TP17773 ILIM5
TP17774 ITP3_DBRESET#
TP17775 ITP3_DBRESET#_R
TP17776 KBC3_A20G
TP17777 KBC3_BKLTON
TP17778 KBC3_BLCKPWRSW#
TP17779 KBC3_CAPSLED#
TP17780 KBC3_CHGEN
TP17781 KBC3_CHKPWRSW#
TP17782 KBC3_CPURST#
TP17783 KBC3_EXTSMI#
TP17784 KBC3_LED_ACIN#
TP17785 KBC3_LED_CHARGE#
TP17786 KBC3_LED_POWER#
TP17787 KBC3_NUMLED#
TP17788 KBC3_PWRBTN#
TP17789 KBC3_PWRGD
TP17790 KBC3_PWRON
TP17791 KBC3_PWRON_INV#
TP17792 KBC3_PWRON_INV#_P1.8V
TP17793 KBC3_PWRON_P1.5V
TP17794 KBC3_PWRSW#
TP17795 KBC3_RSMRST#
TP17796 KBC3_RSMRST#_R_ICH
TP17797 KBC3_RSMRSTF#
TP17798 KBC3_RST#
TP17735 KBC3_RUNSCI#
TP17736 KBC3_SCLED#
TP17737 KBC3_SMCLK#
TP17738 KBC3_SMDATA#
TP17739 KBC3_SPKMUTE_R
TP17740 KBC3_SPKMUTE_RQ_L
TP17741 KBC3_SPKMUTE_RQ_R
TP17742 KBC3_SUSPWR
TP17743 KBC3_THERM_SMCLK
TP17744 KBC3_THERM_SMDATA
TP17745 KBC3_VRON
TP17746 KBC3_WAKESCI#
TP17747 KBC5_KSI(0)
TP17748 KBC5_KSI(1)
TP17749 KBC5_KSI(2)
TP17750 KBC5_KSI(3)

TP17751 KBC5_KSI(4)
TP17752 KBC5_KSI(5)
TP17753 KBC5_KSI(6)
TP17754 KBC5_KSI(7)
TP17755 KBC5_KSO(0)
TP17756 KBC5_KSO(1)
TP17757 KBC5_KSO(10)
TP17758 KBC5_KSO(11)
TP17759 KBC5_KSO(12)
TP17760 KBC5_KSO(13)
TP17761 KBC5_KSO(14)
TP17762 KBC5_KSO(15)
TP17763 KBC5_KSO(2)
TP17764 KBC5_KSO(3)
TP17765 KBC5_KSO(4)
TP17766 KBC5_KSO(5)
TP17719 KBC5_KSO(6)
TP17720 KBC5_KSO(7)
TP17721 KBC5_KSO(8)
TP17722 KBC5_KSO(9)
TP17723 KBC5_TCLK
TP17724 KBC5_TDATA
TP17725 LCD3_BKLTON
TP17726 LCD3_BRIT
TP17727 LED3_AMBER
TP17728 LED3_GREEN
TP17729 LED3_POWERLED
TP17730 LPC3_LAD(0)
TP17731 LPC3_LAD(1)
TP17732 LPC3_LAD(2)
TP17733 LPC3_LAD(3)
TP17734 LPC3_LFRAME#
TP17713 MAX8734_BST3
TP17714 MAX8734_BST5
TP17715 MAX8734_FB3
TP17716 MAX8734_SKIP#
TP17717 MAX8734_THM3_STP#_QQ
TP17718 MAX8734_VCC

DRAW: SUNXIAO,	DATE: 9/10/2007	TITLE: Gevena TEST POINT	SAMSUNG ELECTRONICS
CHECK: WUSHIJIANG,	DEV. STEP: PV2		
APPROVAL: KEVIN_LEE,	REV: 1.0		PART NO.: BA41-undefined
MODULE CODE:	LAST EDIT: October 23, 2007 10:38:02 AM	PAGE 59 OF 59	

TP18605 MCH1_HRCOMP_R
TP18606 MCH1_HSCOMP#_R
TP18607 MCH1_HSCOMP_R
TP18608 MCH1_HVREF
TP18609 MCH1_HXSWING
TP18610 MCH1_VTTLF1_C
TP18611 MCH1_VTTLF2_C
TP18585 MCH1_VTTLF_3_C
TP18586 MCH3_BMBUSY#
TP18587 MCH3_CLKREQ#
TP18588 MCH3_CL_VREF
TP18589 MCH3_EXTTSO#
TP18590 MCH3_EXTTSI#
TP18591 MCH3_ICHSYNC#
TP18592 MCH3_ICHSYNC#_R
TP18593 MCH_TEST1_R
TP18594 MCH_TEST2_R
TP18595 MDC3_BCLK
TP18596 MDC3_RST#
TP18597 MDC3_SDI1
TP18598 MDC3_SDI1_R
TP18599 MDC3_SDO
TP18600 MDC3_SYNC
TP18537 MEM1_SA1_R
TP18538 MEM1_VREF
TP18539 MIN3_CLKREQ#

TP18541 MODEM_TIP_BCON

TP19069 SPI3_CLK
TP19070 SPI3_CLK_R_ICH
TP19071 SPI3_CS0#
TP19072 SPI3_CS1#
TP19073 SPI3_MISO
TP19074 SPI3_MOSI
TP19075 SPI3_MOSI_R_ICH
TP19076 SPK5_L+
TP19077 SPK5_L-
TP19078 SPK5_R+
TP19079 SPK5_R-
TP19080 SUB_BUTTON_L
TP19081 SUB_BUTTON_R
TP19082 SUB_HDD3_LED#
TP19083 SUB_KBC3_CAPSLED#
TP19084 SUB_KBC3_NUMLED#
TP19085 SUB_KBC3_PWRON_INV#
TP19086 SUB_KBC3_SCLED#
TP19087 SUB_LED3_AMBER
TP19088 SUB_LED3_GREEN
TP19089 SUB_LED3_POWERLED
TP19090 SUB_SIO3_CTS1#
TP19091 SUB_SIO3_DCD1#
TP19092 SUB_SIO3_DSR1#
TP19093 SUB_SIO3_DTR1#
TP19094 SUB_SIO3_RI1#
TP19095 SUB_SIO3_RTS1#
TP19096 SUB_SIO3_RXD1
TP19097 SUB_SIO3_TXD1
TP19098 SUB_SIO9_CTS#
TP19099 SUB_SIO9_DCD#
TP19100 SUB_SIO9_DSR#
TP19056 SUB_SIO9_DTR#
TP19057 SUB_SIO9_RI#
TP19058 SUB_SIO9_RTS#
TP19059 SUB_SIO9_RXD
TP19060 SUB_SIO9_TXD
TP19063 SUB_WLON_LED#
TP19064 SYS_SHDN#
TP19065 THM3_ALERT#
TP19066 THM3_STP#
TP19067 TOUCHPAD_BUTTON_L
TP19068 TOUCHPAD_BUTTON_R
TP18247 VCCA_3GP
TP18248 VCCSATAPLL
TP18249 VCC_DMIPLL_L
TP18250 VCC_HPLL

TP18612 P1.25V_M_VCC_AXD
TP18613 P1.5V_CRT_TVDAC
TP18614 P1.5V_GLAN_COMPIO_R
TP18615 P1.8V_AUX_RCOMP#_R
TP18616 P1.8V_AUX_RCOMP_R
TP18617 P1.8V_AUX_RCOMP_VOH_R
TP18618 P1.8V_AUX_RCOMP_VOL_R
TP18619 P1.8V_AUX_VCC_SM_CK
TP18620 P5.0V_ALW_5REF_SUS
TP18621 P5.0V_AUX_BST
TP18622 P5.0V_AUX_HG
TP18623 P5.0V_AUX_LG
TP18624 P5.0V_AUX_PHASE
TP18625 P5.0V_VSREF
TP18626 PCI3_CLKRUN#
TP18627 PCI3_DEVSEL#
TP18628 PCI3_FRAME#
TP18629 PCI3_GNT0#
TP18630 PCI3_INTA#
TP18631 PCI3_INTB#
TP18632 PCI3_INTC#
TP18633 PCI3_INTD#
TP18634 PCI3_INTE#
TP18635 PCI3_INTF#
TP18636 PCI3_INTG#
TP18637 PCI3_INTH#
TP18067 PCI3_IRDY#
TP18068 PCI3_PERR#
TP18069 PCI3_PLOCK#
TP18070 PCI3_REQ0#
TP18071 PCI3_SERR#
TP18072 PCI3_STOP#
TP18073 PCI3_TRDY#

TP18053 PEX3_WAKE#
TP18054 PLT3_RSTF#_MCH_R

TP18057 SC452_CS1-
TP18021 SC452_HYS
TP18022 SC452_BST1
TP18023 SC452_BST2
TP18024 SC452_BST2_RC
TP18025 SC452_CS2+
TP18026 SC452_CS2-
TP18027 SC452_DAC
TP18028 SC452_DPRSLP
TP18029 SC452_DPRSTP#
TP18030 SC452_DRP+
TP18031 SC452_DRP-
TP18032 SC452_ERROUT
TP18033 SC452_FB+
TP18034 SC452_FB-
TP18035 SC452_ISH
TP18036 SC452_SS
TP18037 SC452_VPN1
TP18038 SC452_VPN2
TP18039 SC452_VREF
TP18040 SIO3_CTS1#
TP18041 SIO3_DCD1#
TP18042 SIO3_DSR1#
TP18043 SIO3_DTR1#
TP18044 SIO3_RI1#
TP18045 SIO3_RTS1#
TP18046 SIO3_RXD1
TP18047 SIO3_TXD1
TP18048 SMB3_ALERT#
TP18049 SMB3_CLK
TP18050 SMB3_DATA
TP18051 SMB3_ME_CLK
TP18052 SMB3_ME_DATA

TP19054 VRM3_CPU_PWRGD
TP19055 VTT3_PWRGD
TP18230 WLON_LED#
TP18232 G.7VDDQA
TP18235 CHG_REF
TP18241 GND2
TP18242 GND2
TP18245 G_AUD
TP18198 G_CHG
TP18200 G_CPU
TP18204 G_DDR
TP18208 G_P1.25V
TP18212 G_P1.5V
TP18217 G_P3.3V
TP18222 LCD_VDD3V
TP18223 LCD_VDD3V
TP18224 LDO_P5.4V
TP18225 LDO_P5.4V
TP18116 PRTC_BAT
TP18122 TMDS_PLLVDD
TP18124 VCCP_CORE
TP18125 VCCP_CORE
TP18130 VCC_CRT
TP18131 VCC_CRT
TP18081 VDC
TP18084 VDC_ADPT
TP18089 VDC_INV
TP18095 VDD_AMP
TP18098 VDD_AUD

TP18164 P0.9V
TP18170 P1.05V_PEG
TP18172 P1.25V
TP18178 P1.2V
TP18183 P1.5V
TP18187 P1.5V_EXP
TP18188 P1.8V
TP18192 P1.8V_AUX
TP18134 P12.0V_ALW
TP18136 P3.3V_AUX
TP18141 P3.3V_AUX_EXP
TP18146 P3.3V_EXP
TP18150 P3.3V_MCD
TP18152 P3.3V_MICOM
TP18158 P3.3V_SUB
TP18161 P5.0V_ALW
TP18104 P5.0V_AUX
TP18109 P5.0V_SIO
TP18112 P5.0V_USB

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CHECK: WUSHIJIANG,	DEV. STEP: PV2		
APPROVAL: KEVIN_LEE,	REV: 1.0		PART NO.: BA41-undefi
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